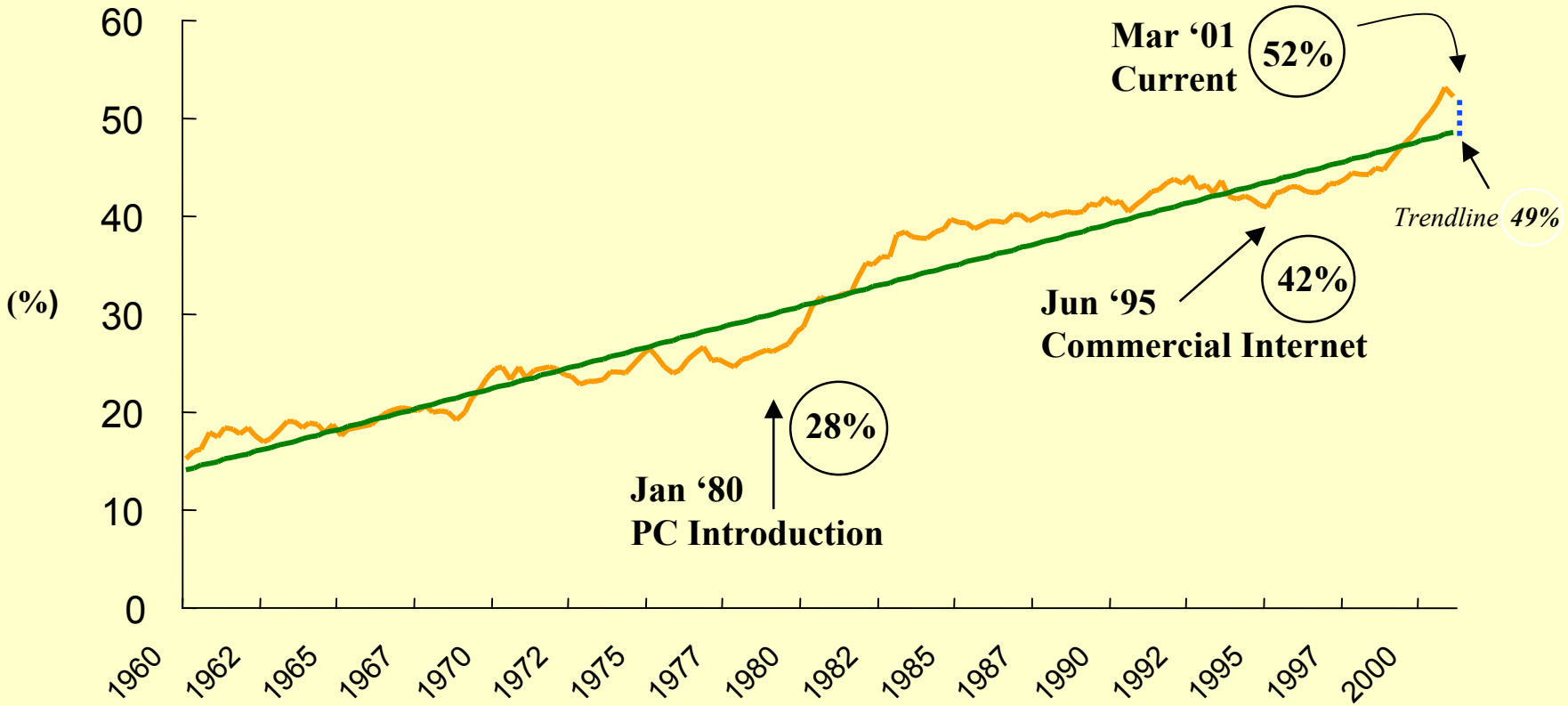
CYPRESS SEMICONDUCTOR CORPORATION

COMMUNICATIONS DESIGN CONFERENCE
SEPTEMBER 24, 2002

T.J. RODGERS
PRESIDENT & CEO

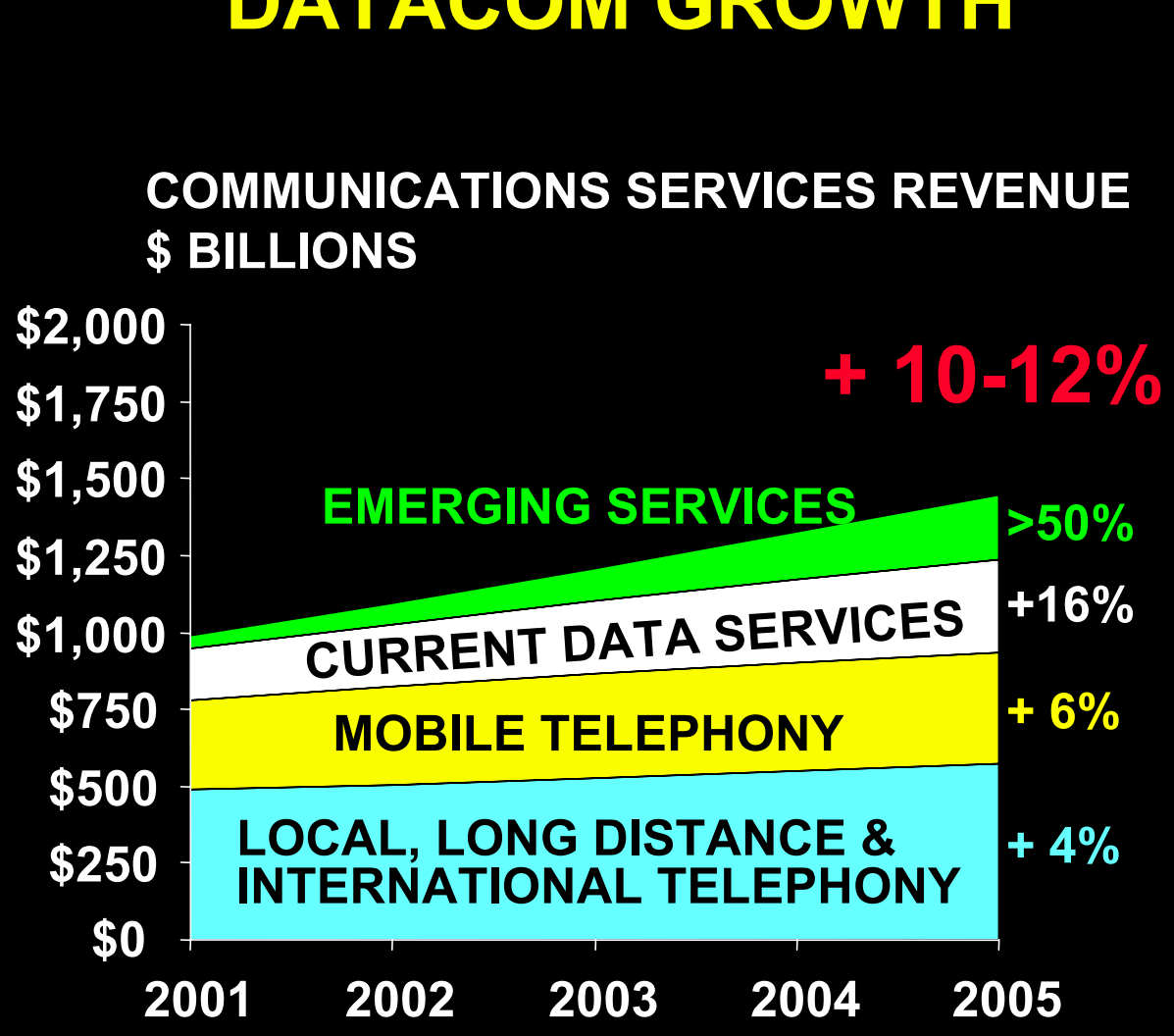
Tech Spending Has Risen Rapidly and Has Been Above Trend line

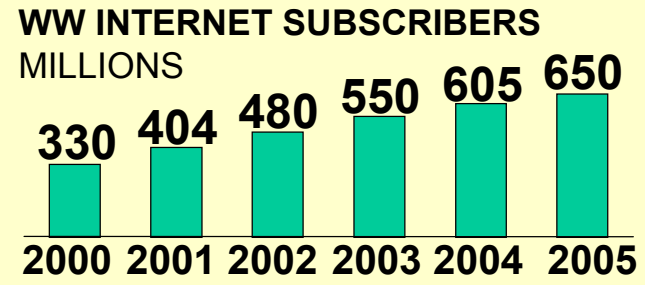
U.S.-based Information Technology % of Nominal Business Capital Equipment Spending



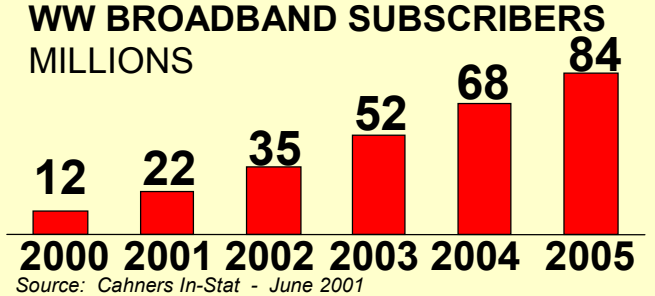
Source: Morgan Stanley Internet Research; Bureau of Economic Analysis; Data as of 05/03/01

DATACOM GROWTH

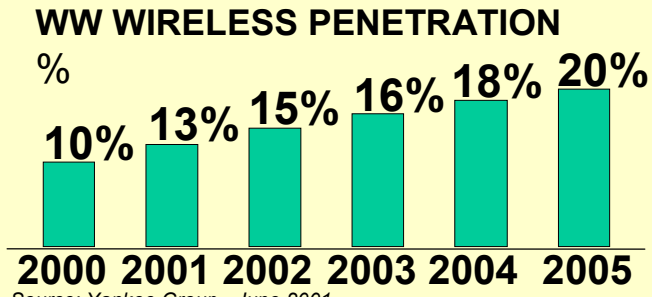




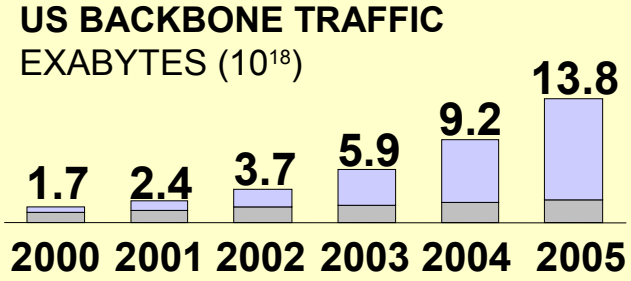
Source: Dataquest - May 2001



Source: Cahners In-Stat - June 2001



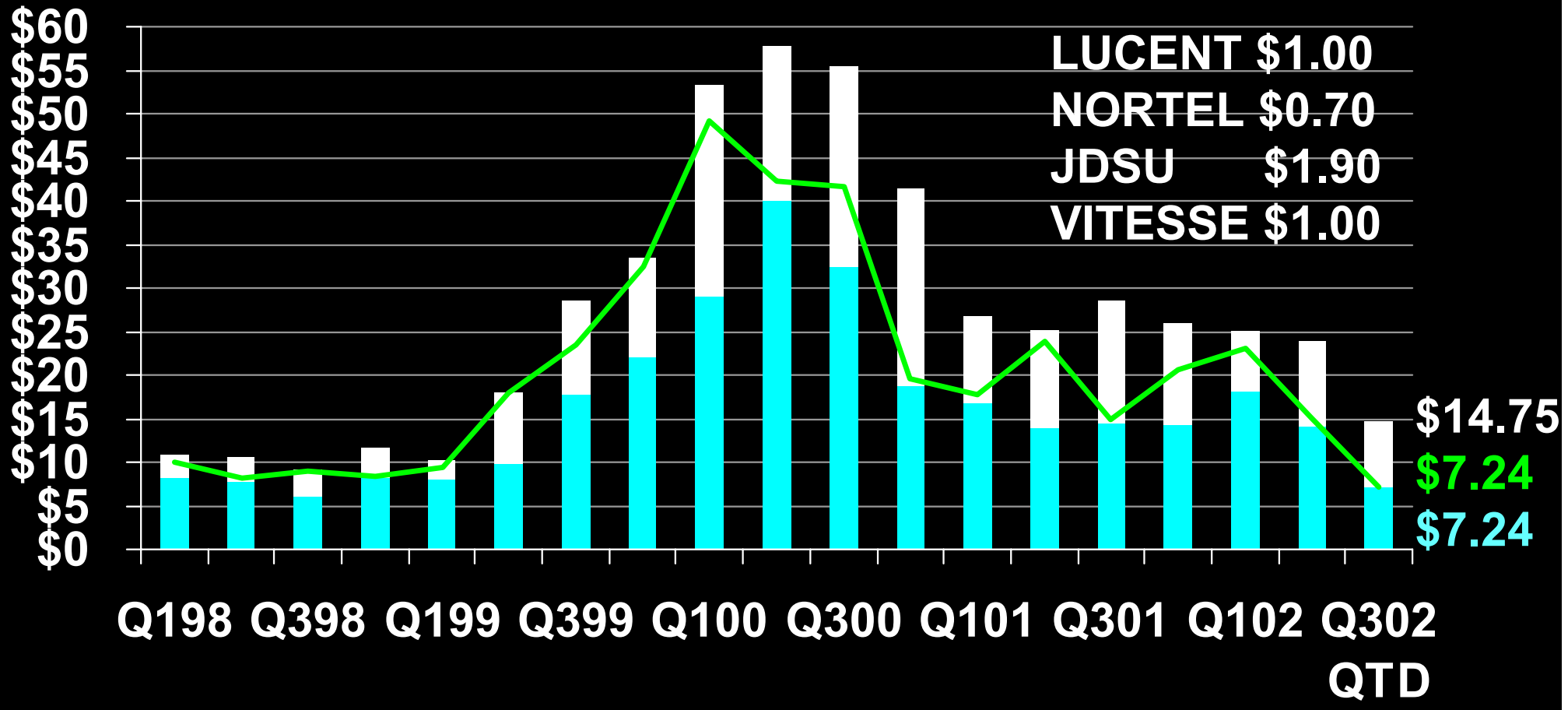
Source: Yankee Group - June 2001



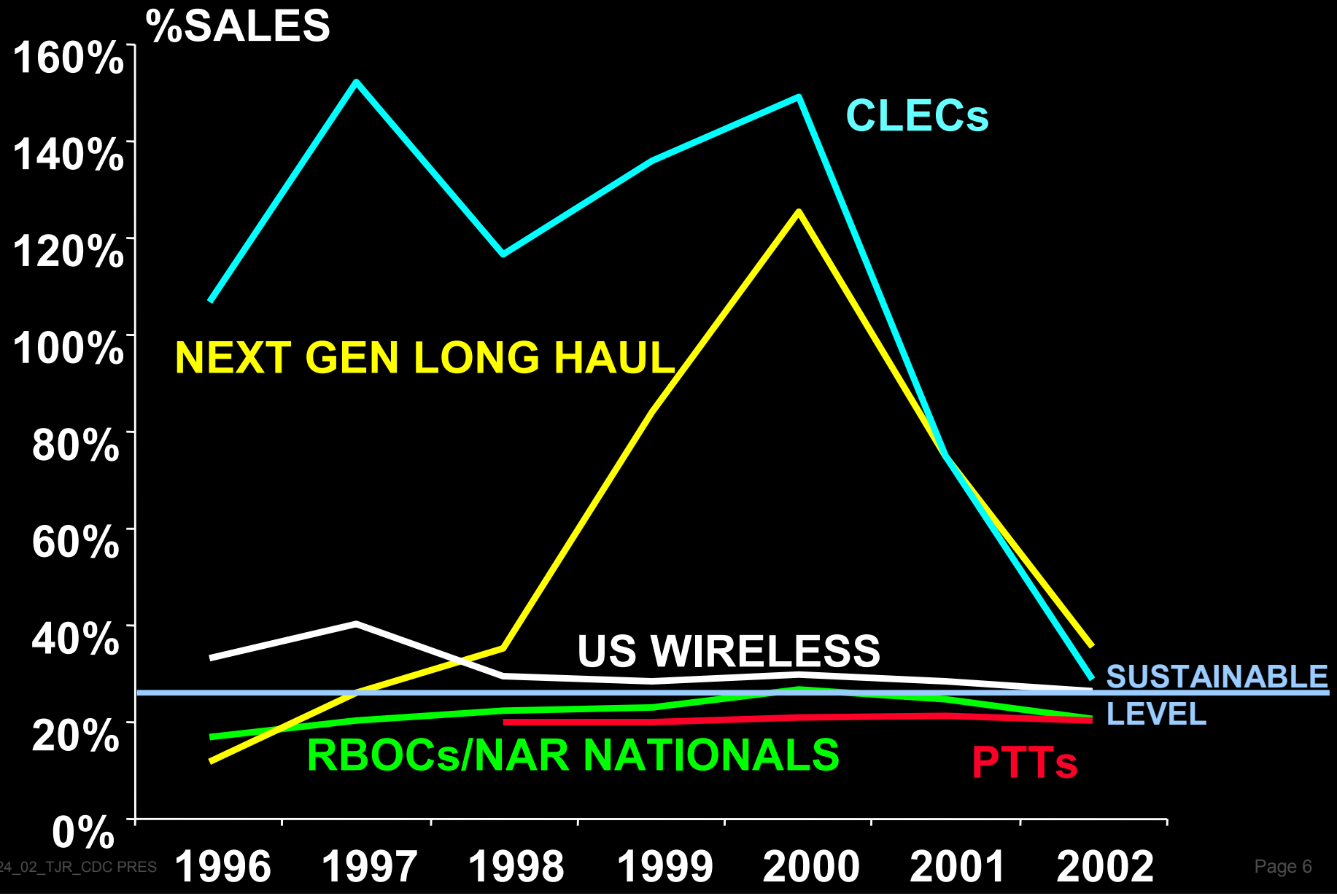
Source: McKinsey & JP Morgan - May 2001


ECONOMY

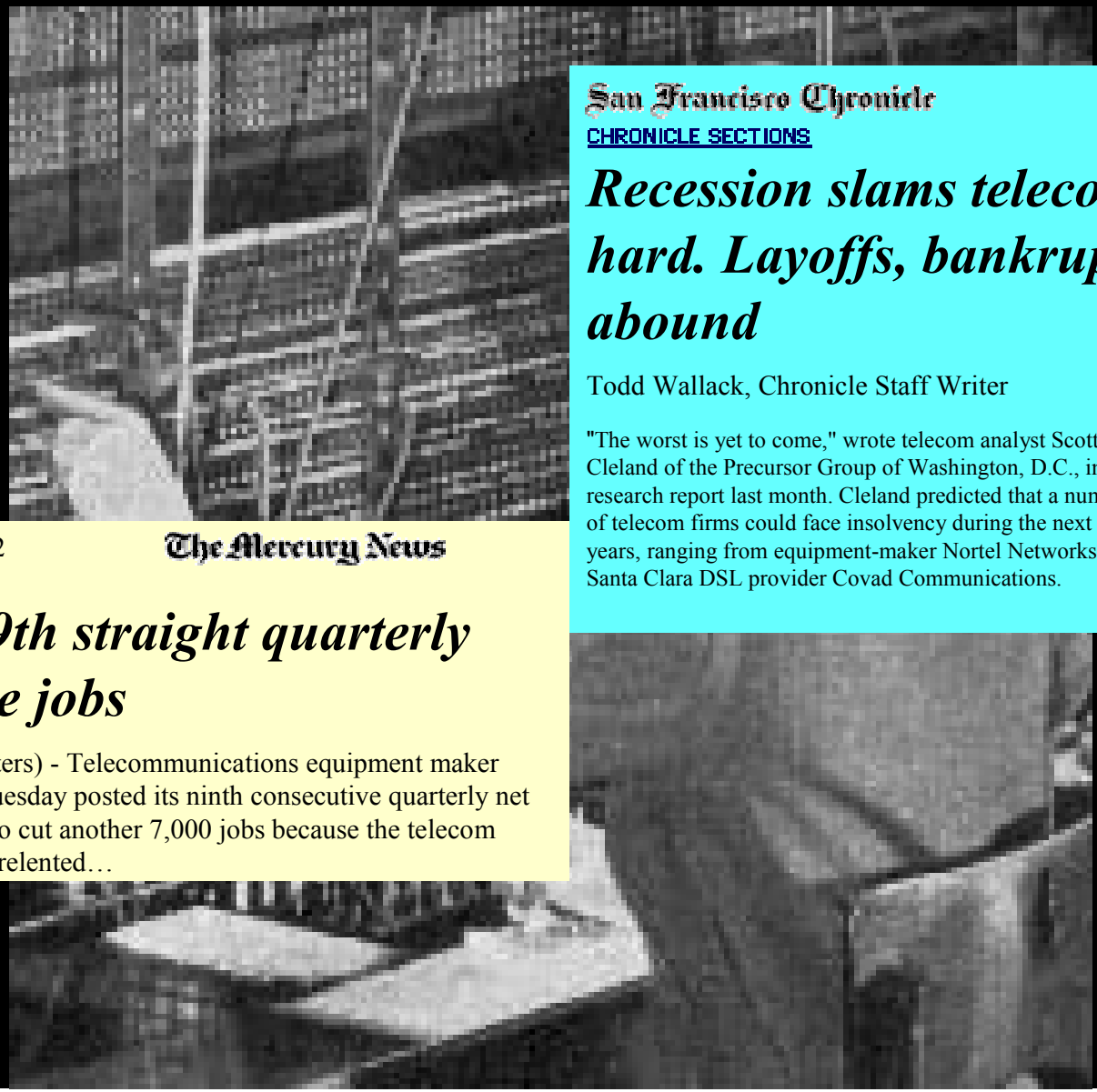
CYPRESS SHARE PRICE



SERVICE PROVIDER CAP-EX



WHY COMMUNICATIONS?



San Francisco Chronicle

CHRONICLE SECTIONS

Recession slams telecoms hard. Layoffs, bankruptcies abound

Todd Wallack, Chronicle Staff Writer

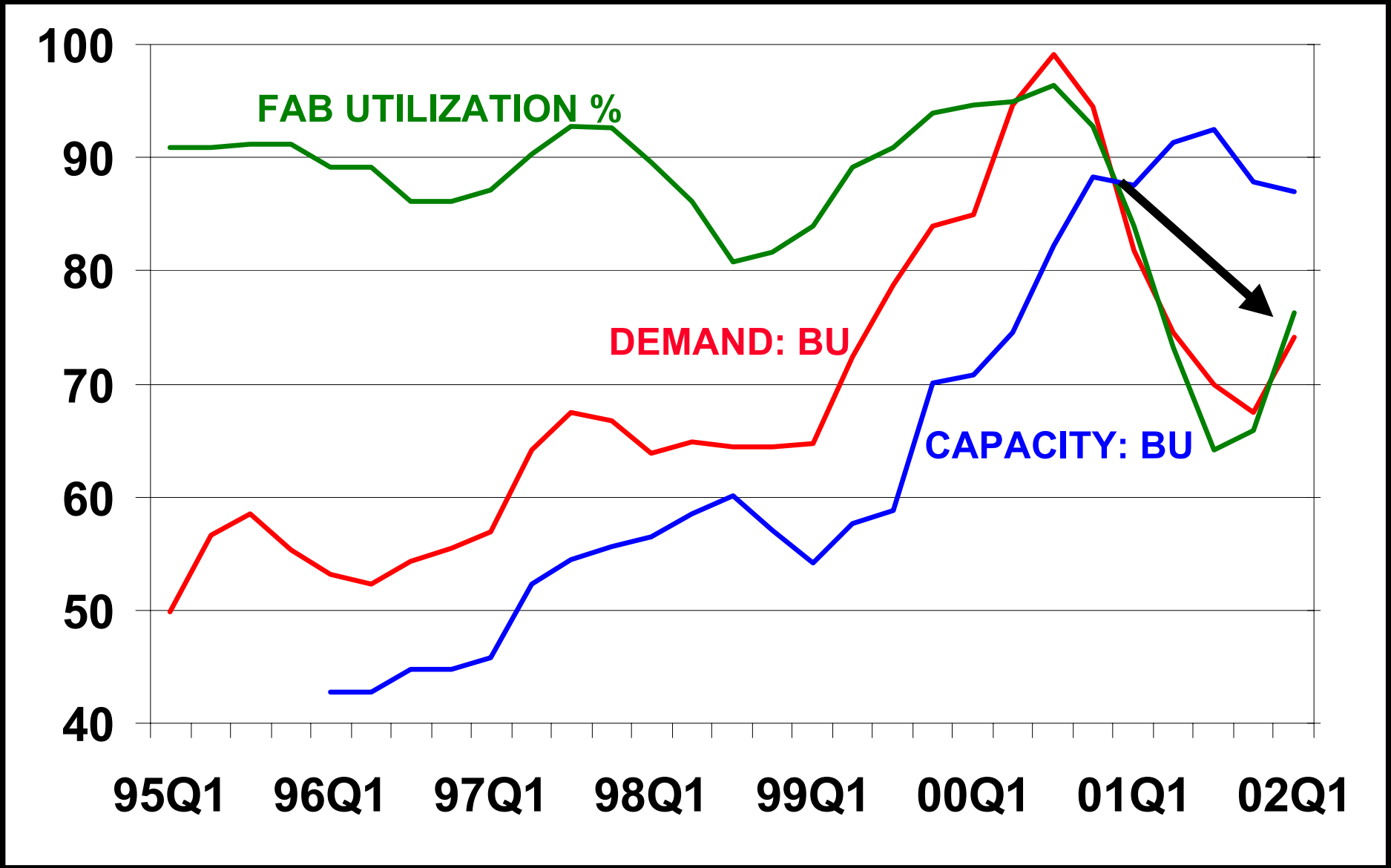
"The worst is yet to come," wrote telecom analyst Scott Cleland of the Precursor Group of Washington, D.C., in a research report last month. Cleland predicted that a number of telecom firms could face insolvency during the next two years, ranging from equipment-maker Nortel Networks to Santa Clara DSL provider Covad Communications.

Posted on Tue, Jul. 23, 2002 The Mercury News

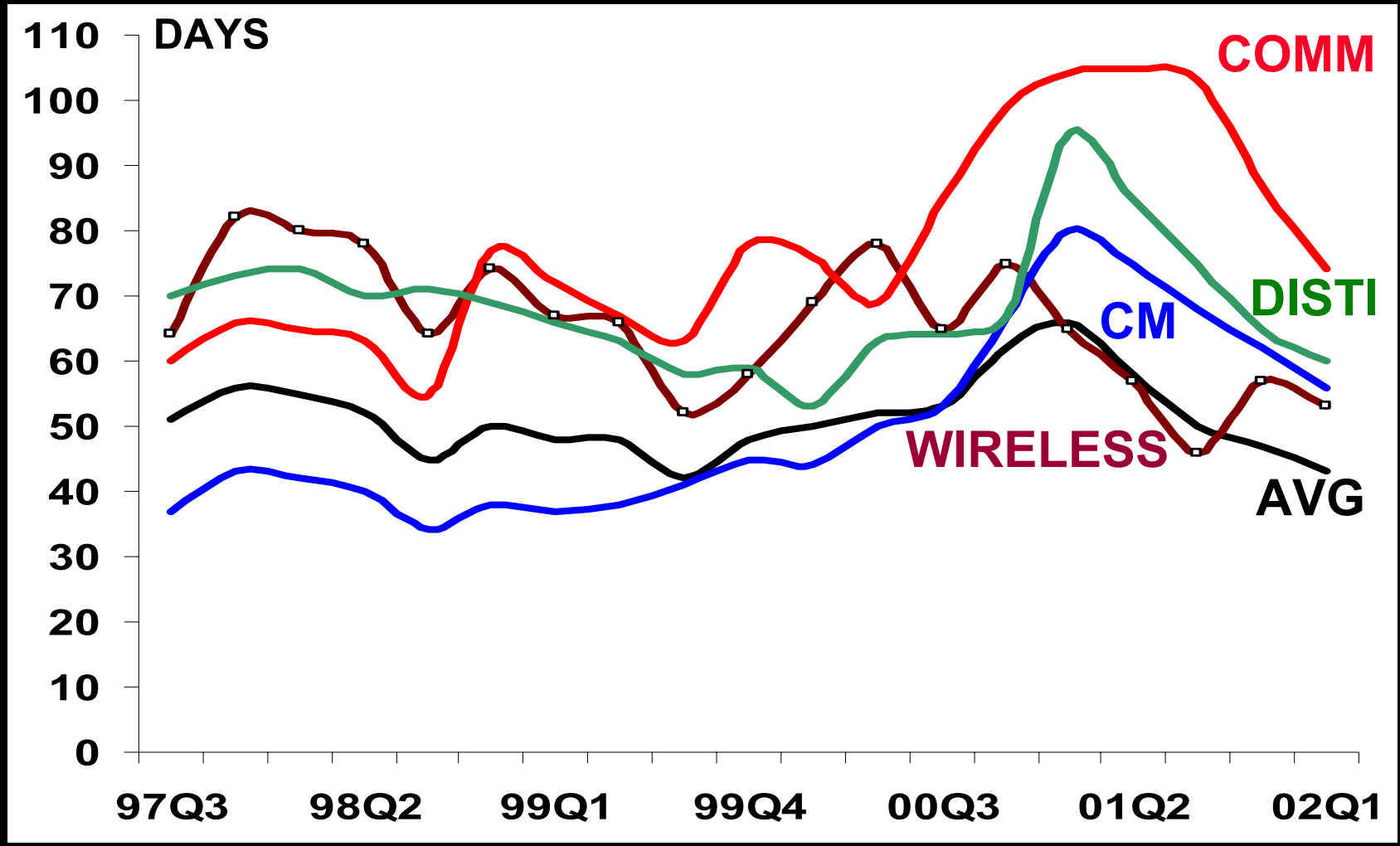
Lucent posts 9th straight quarterly loss, cuts more jobs

MURRAY HILL, N.J. (Reuters) - Telecommunications equipment maker Lucent Technologies Inc. Tuesday posted its ninth consecutive quarterly net loss and said it would have to cut another 7,000 jobs because the telecom spending slowdown has not relented…

SEMICONDUCTOR SUPPLY & DEMAND



CUSTOMER INVENTORY

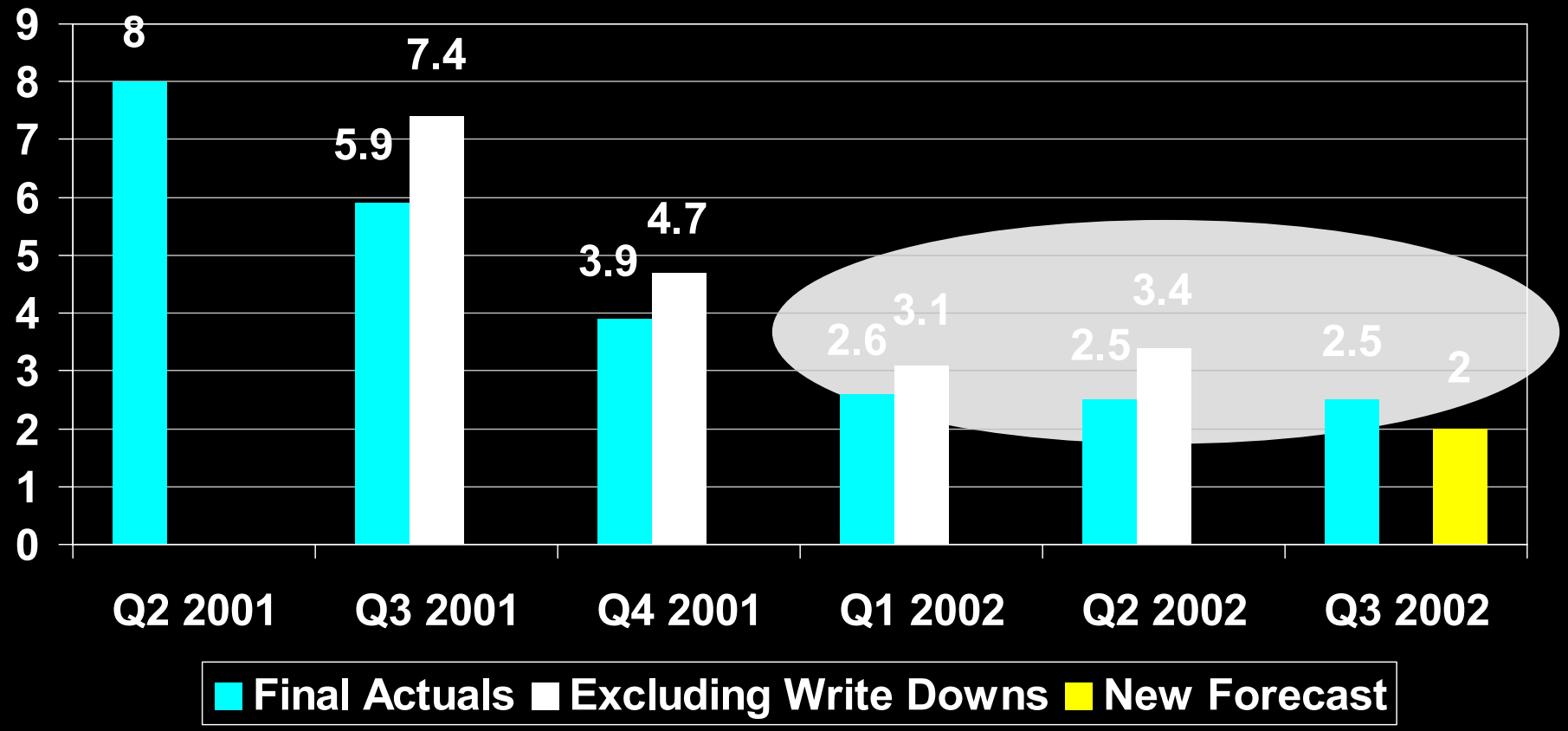


"Near-death experience forces collaboration."

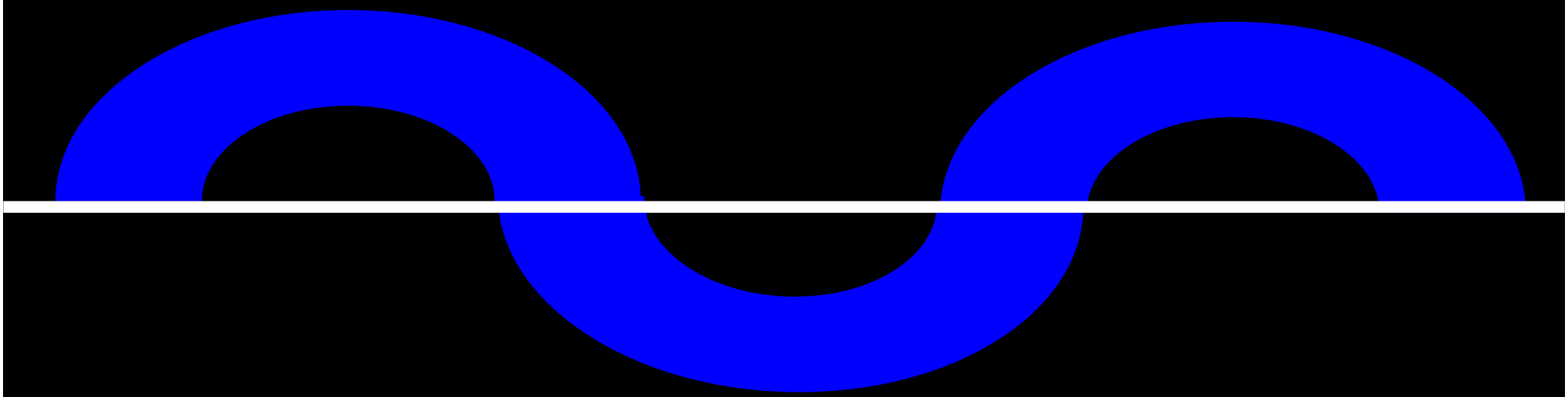
—Dave Ayers
Officer, Supply Chain Engineering
Lucent

EXCESS SEMICONDUCTOR INVENTORY FORECAST

CONSUMPTION OF EXCESS INVENTORY HAS SLOWED AND WRITE-OFFS HAVE INCREASED…



WHERE ARE WE IN THE CYCLE?



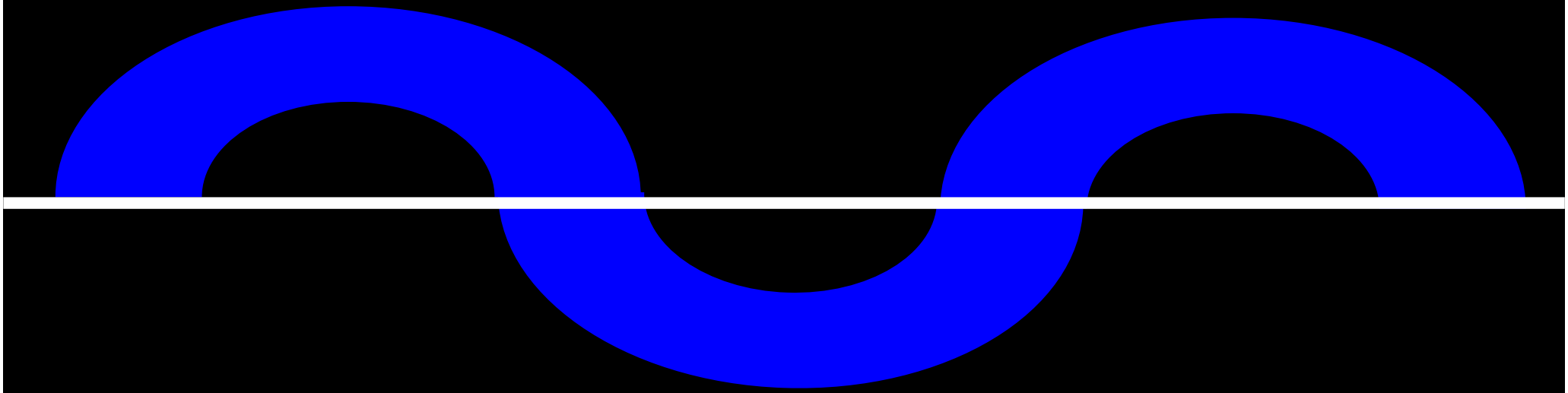
TECHNOLOGY BUYS

CAPACITY BUYS

OVER-BUILD

OVER-INVENTORY

WHERE ARE WE IN THE CYCLE?



TECHNOLOGY BUYS

CAPACITY BUYS

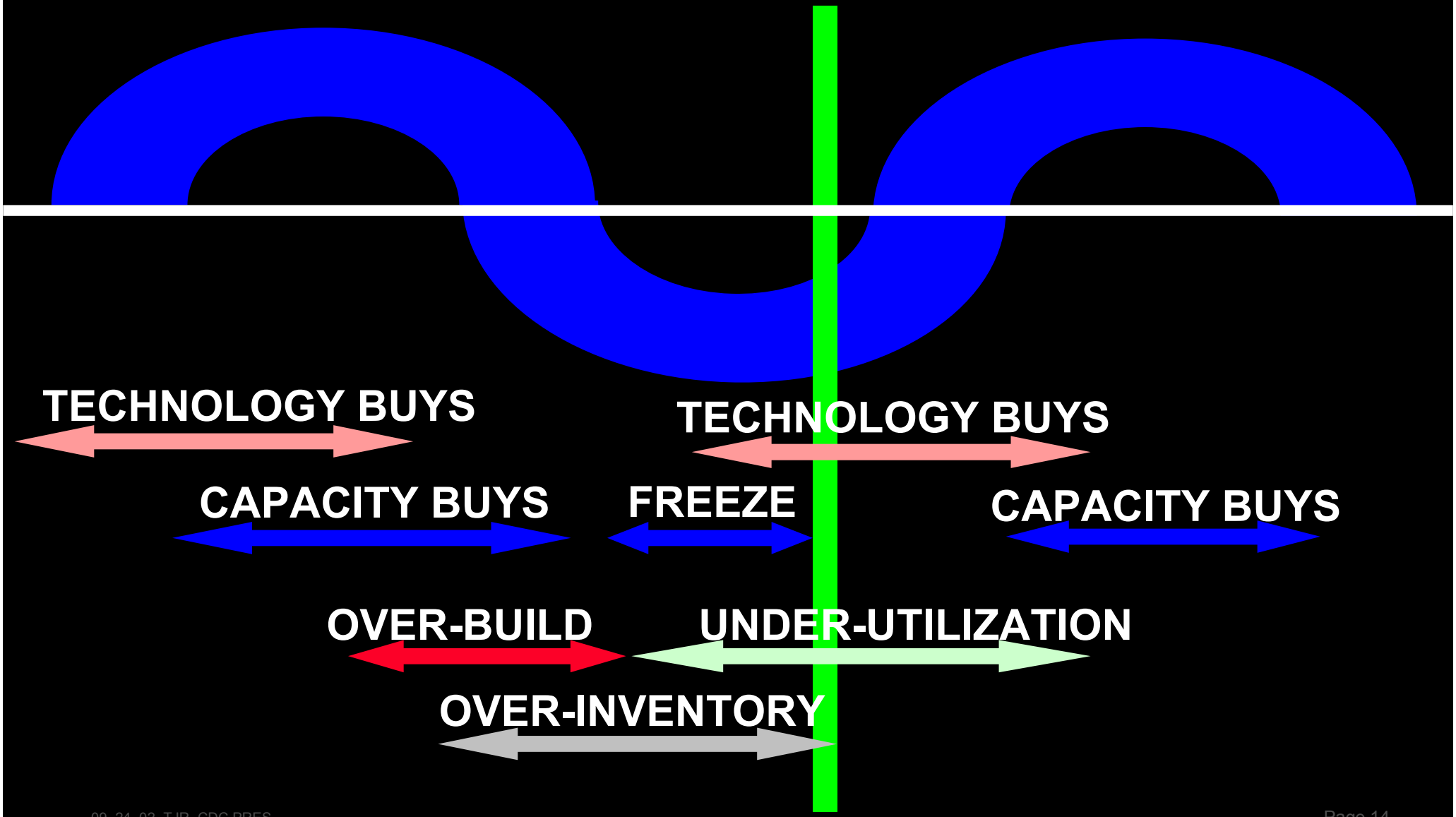
FREEZE

OVER-BUILD

UNDER-UTILIZATION

OVER-INVENTORY

WHERE ARE WE IN THE CYCLE?



HISTORY LESSON:
THE RAILROAD BUBBLE

IN BRITAIN:

1850: 6,084 MILES OF TRACK WHEN BUBBLE BURST

1910: 21,000 MILES OF TRACK

IN US:

1860: 30,000 MILES OF TRACK WHEN BUBBLE BURST

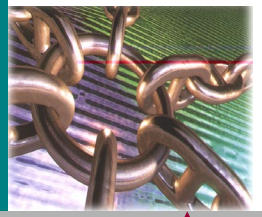
1900: 500,000 MILES OF TRACK

Source: P.J. C. Ransom in I. McNeil, A. Fishlow
Data courtesy of Brian Arthur

"Gee Ed, do you have any idea what this is going to cost?"

Collaborative Design

means more than just working next to each other.



Supplier Partnership Evolution

Product Partnering
- Design collaboration
- Supply chain collaboration
- Full stream cost reduction

Portfolio Planning
- Market trend review
- Technology roadmap definition
- Joint portfolio planning

Design Review
- Supplier partnership workshops
- Product high level definition
- Product level cost reduction

Commodity Sourcing
- Security of supply
- Quality of components
- Component level cost reduction

FLEXTRONICS

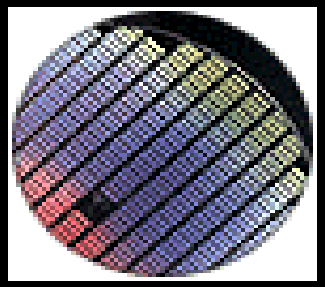
Characteristics of Good Supply Chain Management

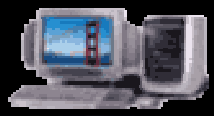
- Price is Not the Only Thing that Matters
- Performance Criteria used to Determine Splits
- Appropriate Payment Terms
- Liability Management
- Respond to Suppliers Needs
- Allow Suppliers to Create Value
  - Supply Chain Integration
  - Logistics Management

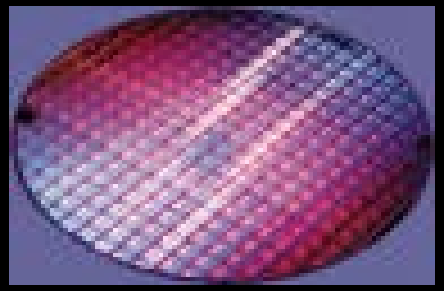
Michael Marks: Keynote Speaker -- First Annual Supply Network Conference, San Jose, California, September 2002

THE ELECTRONICS FOOD CHAIN

SILICON WAFER | IC "CHIPS" | BOARDS | SYSTEMS







AMT → CY CY CY → SYSCO SYSCO SYSCO SYSCO →

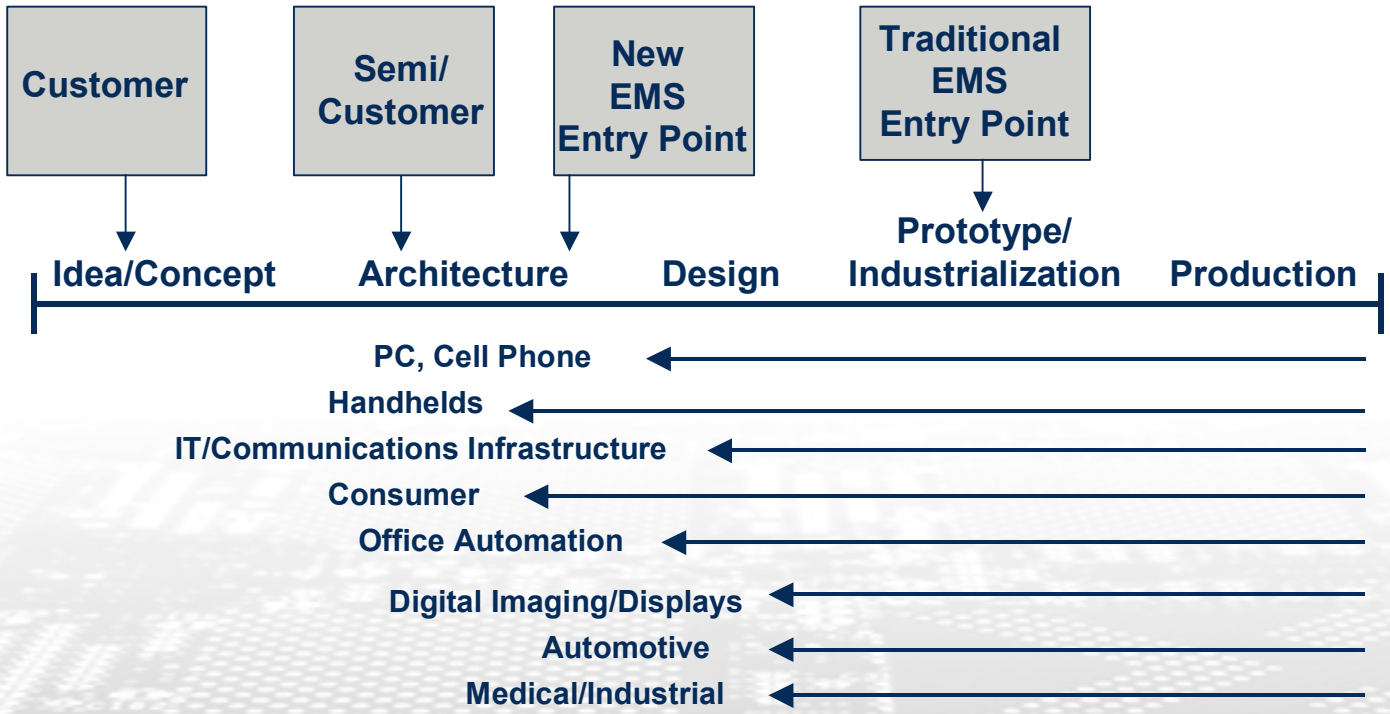
EQUIPMENT | DESIGN | RELIABILITY | SYSTEM INTEGRATION | CUSTOMER

PROCESS | TEST | BOARD DESIGN | SOFTWARE

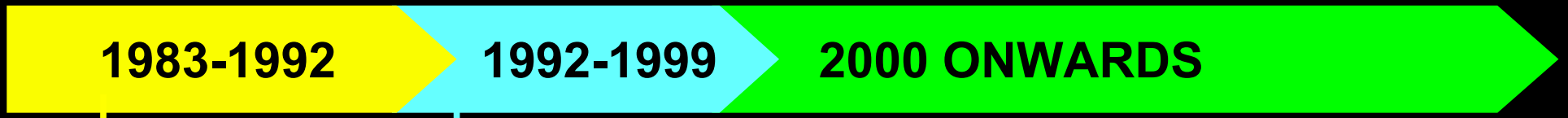
EMS becoming Design Driven

- Engaging earlier in the product life cycle
- OEM Divestitures will continue
- Opportunity to engage with customers earlier in the design cycle

Typical Design Cycle



CYPRESS TRANSFORMATION



MARKET FOCUSED

SUPPORTTING MARKETS (WIRELESS, SAN, WAN)

PRODUCT/MANUFACTURING FOCUSED

BUILDING PRODUCT LINES (MANY CYPRESSES)

TECHNOLOGY FOCUSED

HIGH SPEED CMOS (“INTEL DELIVERS”)

STRATEGIC ACQUISITIONS

		PCD PERSONAL COMM	TTD TIMING PROD	CMS CYPRESS MICRO	SLM SILICON LIGHT
WIT WIN	MOTOROLA 7% NEC 5% INTEL 3% ERICSSON 2%	BLUETOOTH			
WAN SAN	MOTOROLA 7% CISCO 6% NORTEL 4% LUCENT 3% EMC 1% IBM 1% COMPAQ 1%		ROBOCLOCK ZERO DELAY EMI BUFFER ComL		OPTICS O/E CONV
PC CNSMR		USB ECHELON	PROG CLOCK PC CLOCK	PSoC	

GALVANTECH

HIBAND
ARCUS
LARA NET

RADIOCOM
ALATION
ISD
ANCHOR
SCANLOGIC

IC WORKS
IMI

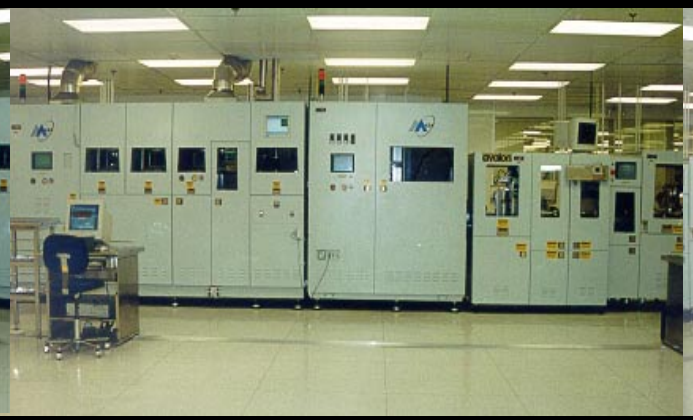
STANDARDS BODIES

MANUFACTURING COOPERATION

PROBLEM: TIME TO MARKET

SOLUTION: AUTOLINE, ASSY & TEST TIME 8 HRS

BENEFIT: FAST RAMP FOR MOBILE MARKET



CONSULTANTS PROGRAM

122 CONSULTANTS APPROVED:

- **PSoC = 100**
- **USB = 22**

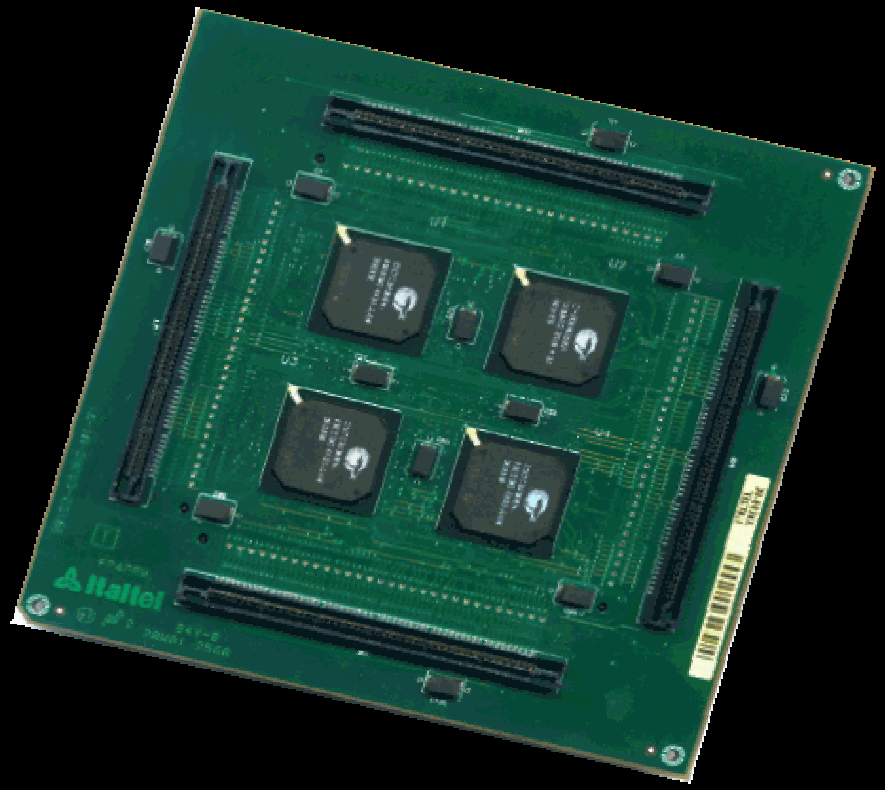
CERTIFICATION & TRAINING PROCESS

COLLABORATIVE WEBSITE LIVE

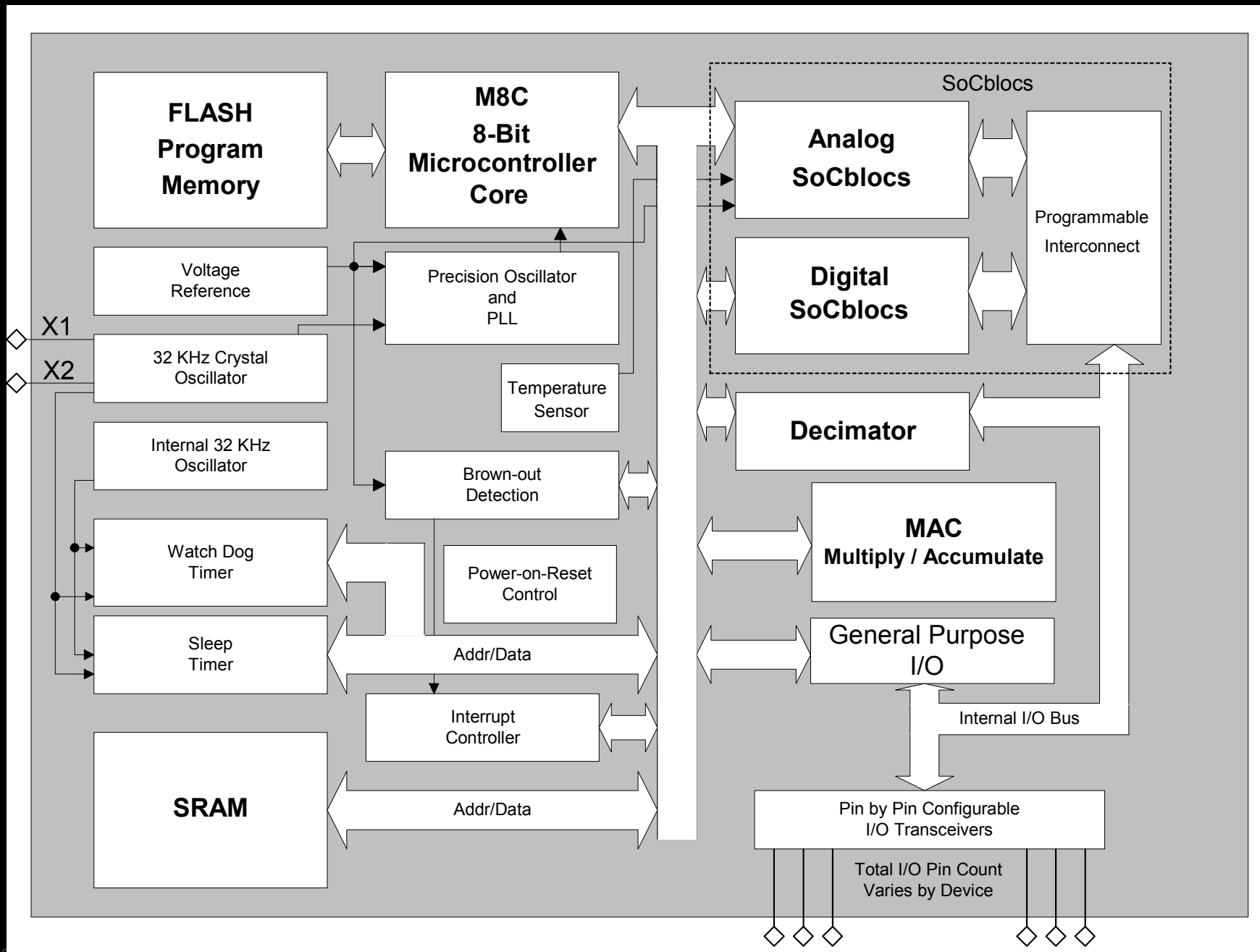
IP PROCESS IN DEFINITION

CDC BOOTH PARTNER

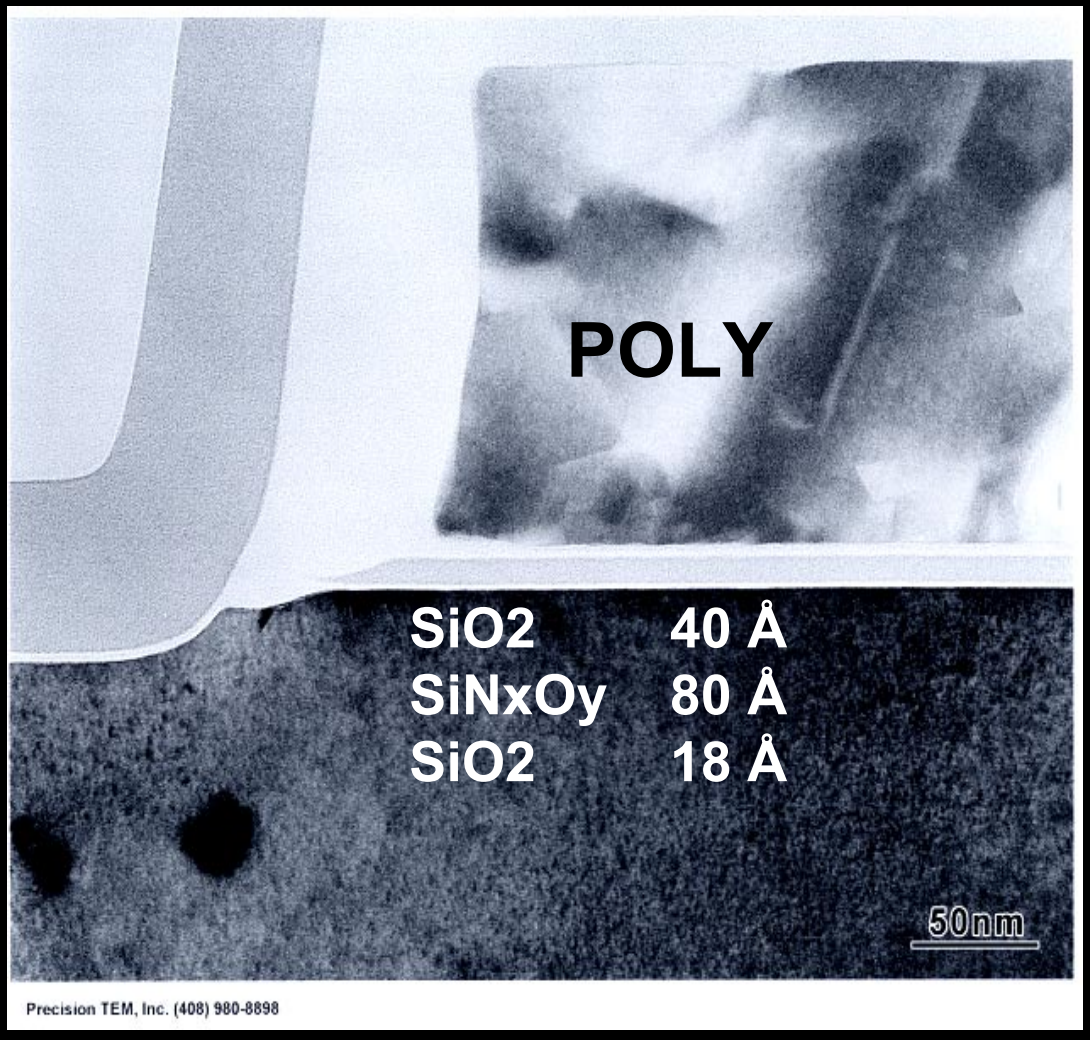
CDC BOOTH PARTNER
ITALTEL FLEXBENCH

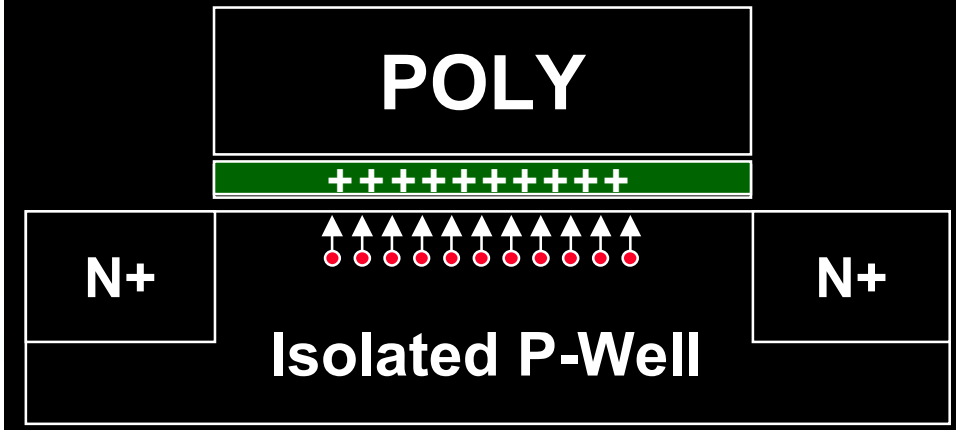


PROBLEM: TIME TO MARKET

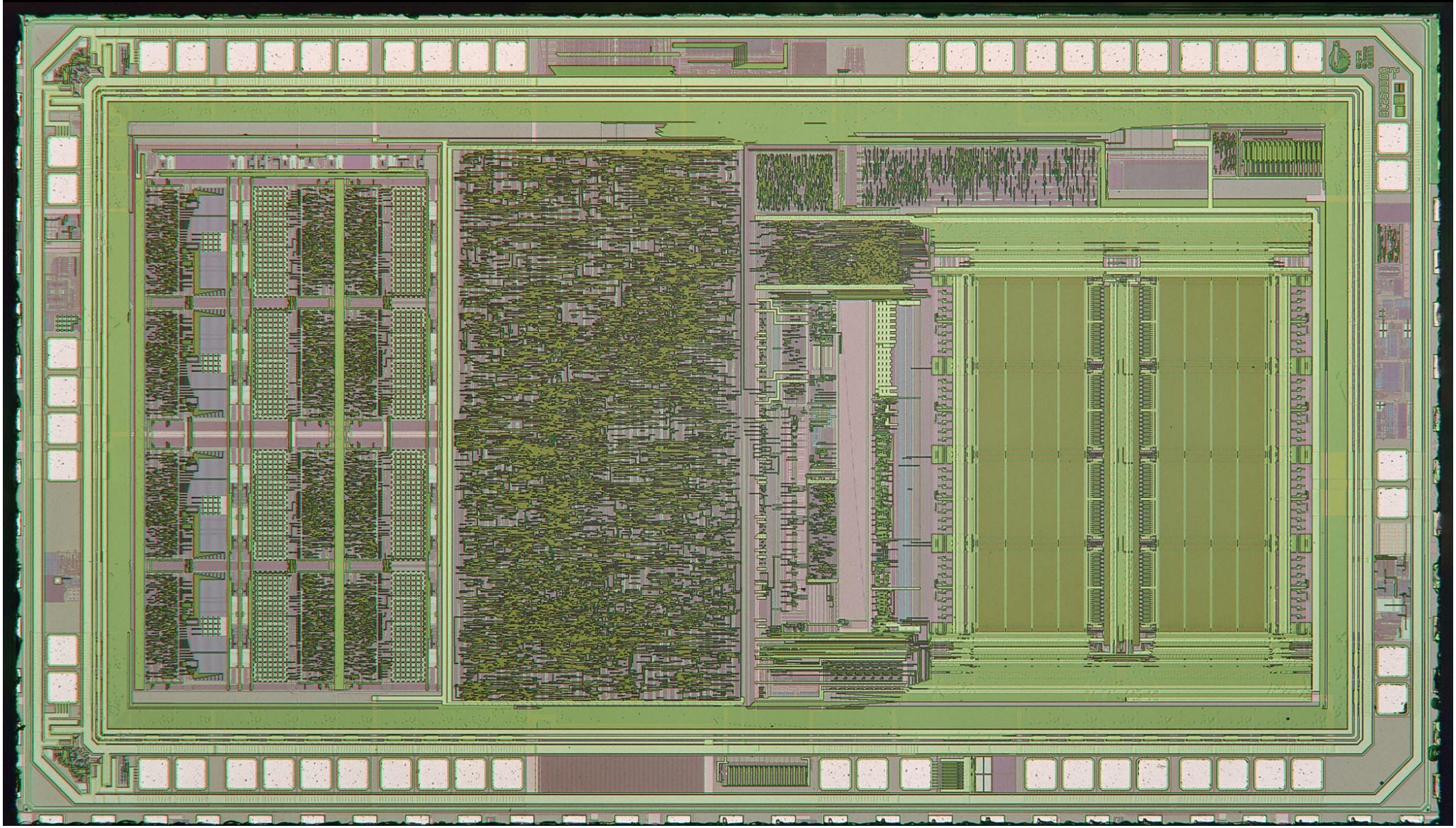

FLASH
Program
Memory
M8C
8-Bit
Microcontroller
Core
SoCblocs
Analog
SoCblocs
Programmable
Interconnect
Digital
SoCblocs
Voltage
Reference
Precision Oscillator
and
PLL
X1
X2
32 KHz Crystal
Oscillator
Temperature
Sensor
Internal 32 KHz
Oscillator
Decimator
Brown-out
Detection
MAC
Multiply / Accumulate
Watch Dog
Timer
Power-on-Reset
Control
Sleep
Timer
Addr/Data
General Purpose
I/O
Internal I/O Bus
Interrupt
Controller
SRAM
Addr/Data
Pin by Pin Configurable
I/O Transceivers
Total I/O Pin Count
Varies by Device

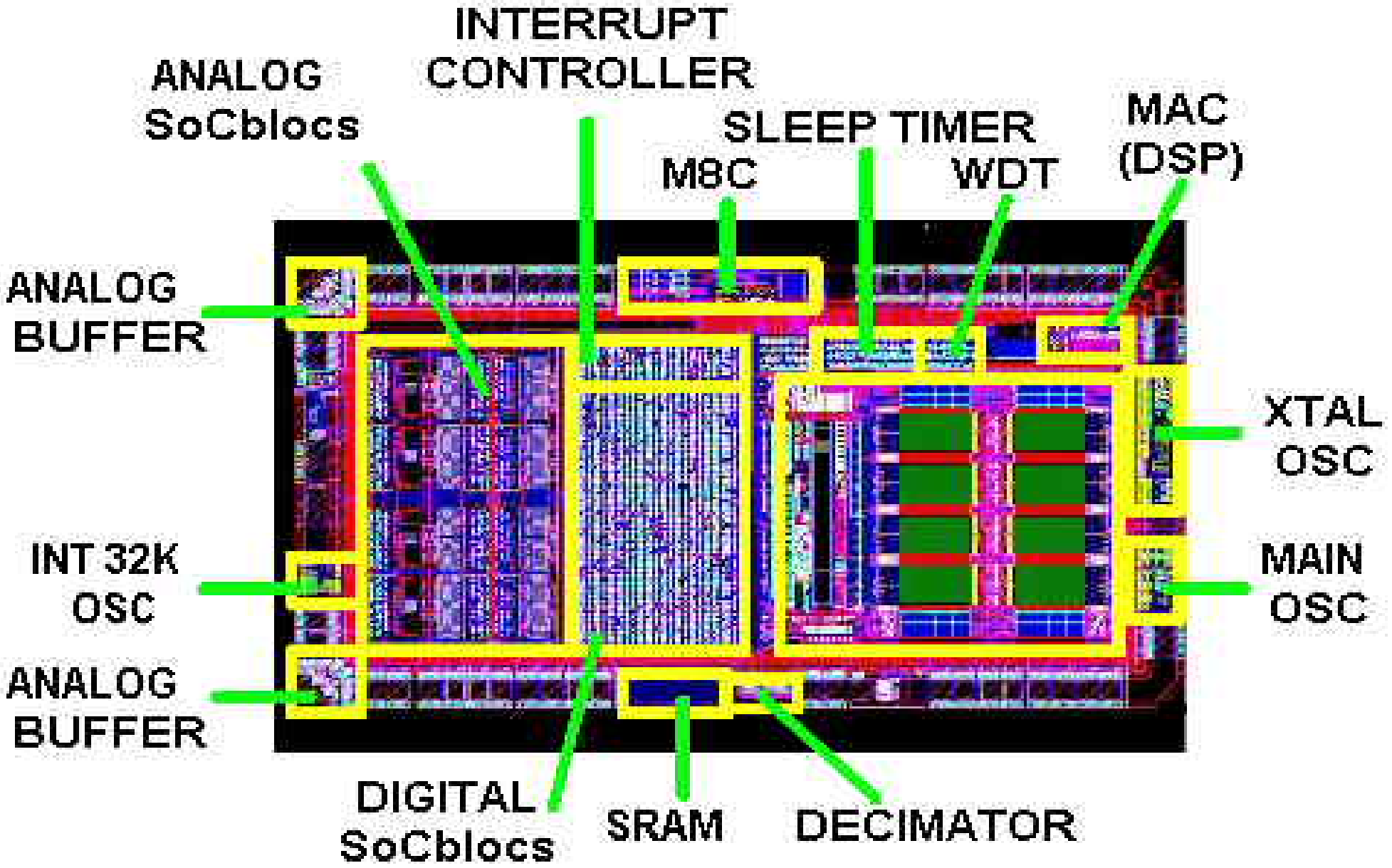
SONOS DEVICE





PSoC DIE

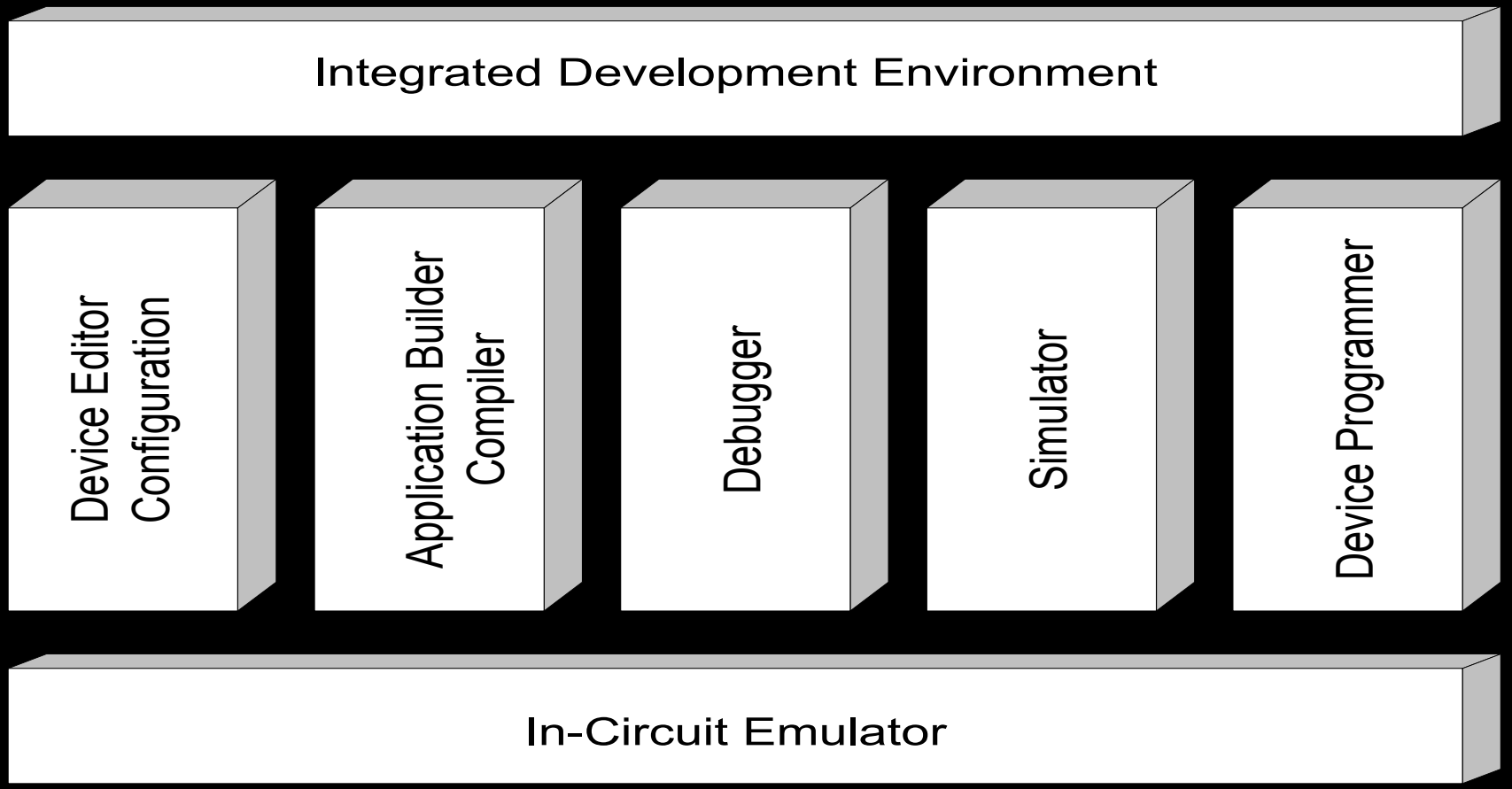



INTERRUPT
CONTROLLER
ANALOG
SoCblocs
SLEEP TIMER
M8C
WDT
MAC
(DSP)
ANALOG
BUFFER
XTAL
OSC
INT 32K
OSC
MAIN
OSC
ANALOG
BUFFER
DIGITAL
SoCblocs
SRAM
DECIMATOR

ANALOG CAPABILITY

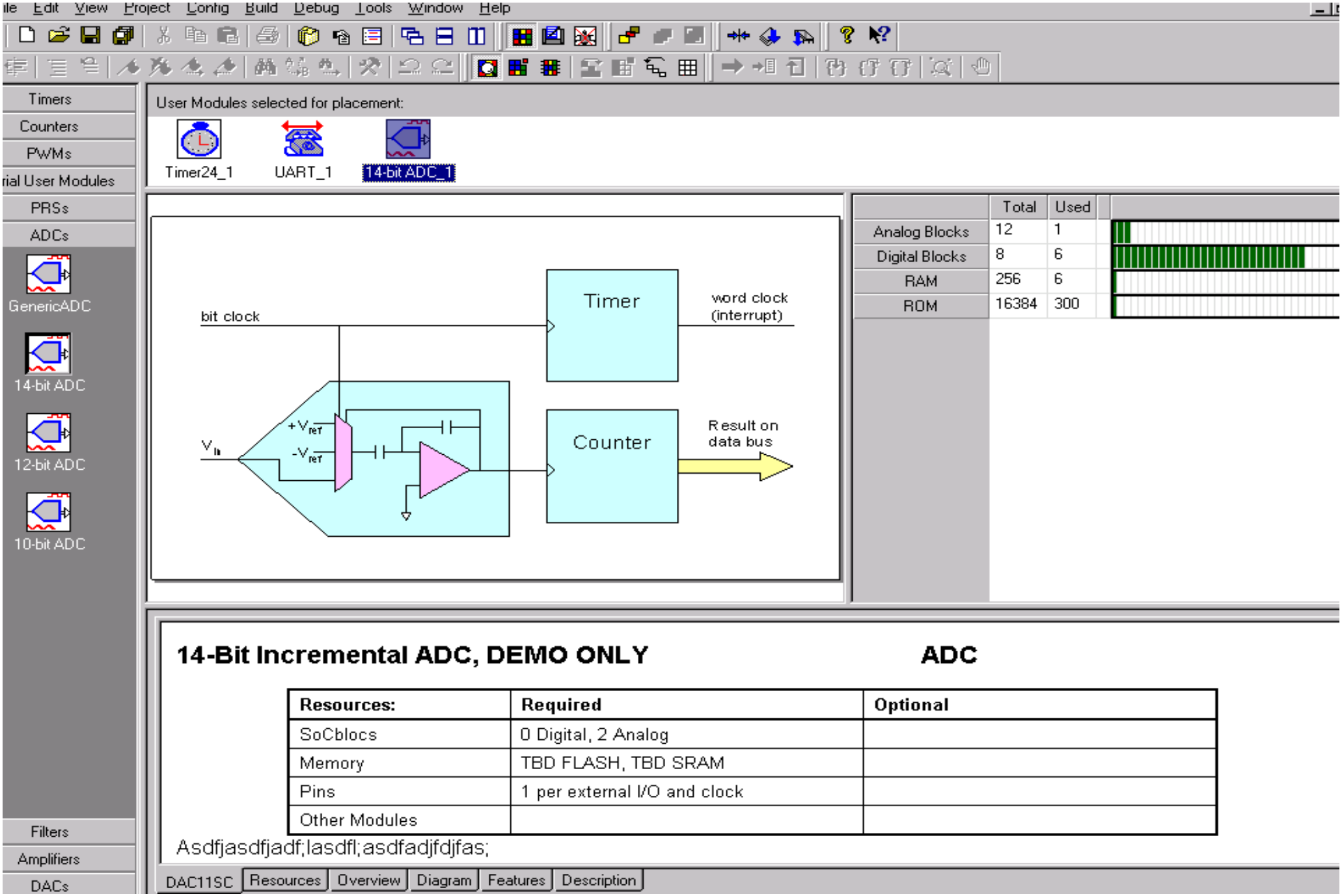
- Delta-Sigma A/D converters
- Successive Approximation A/D converters
- Incremental A/D converters
- Programmable gain/loss stage
- Analog comparators
- Zero-crossing detectors
- Filters
- Amplitude modulators,
- Amplitude demodulators
- Sine-wave generators
- Sine-wave detectors
- Sideband detection
- Sideband stripping
- Frequency modulation
- Frequency demodulation
- Audio coding, audio decoding,
- Audio output drive
- Audio compress/expansion

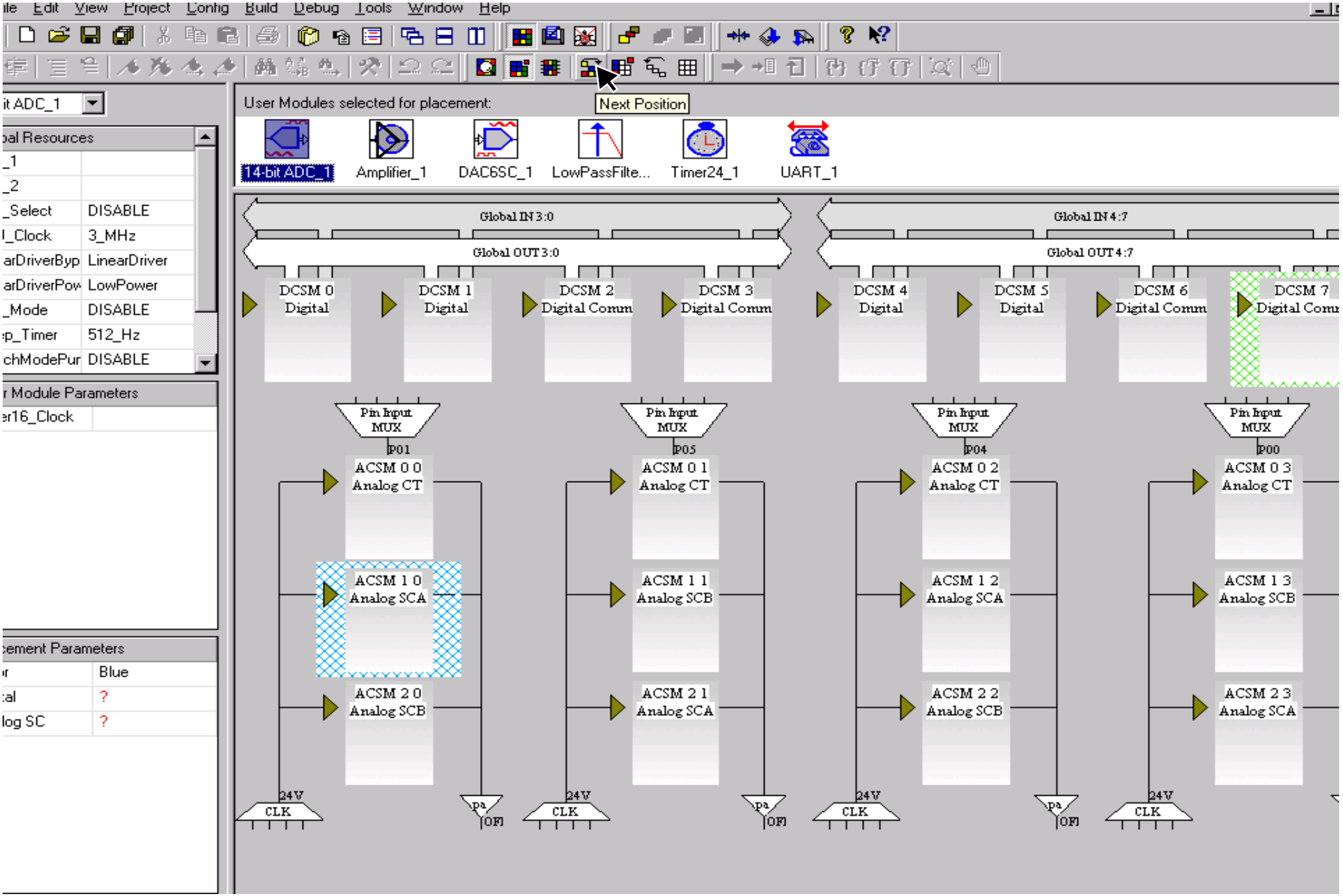
PSoC Designer™

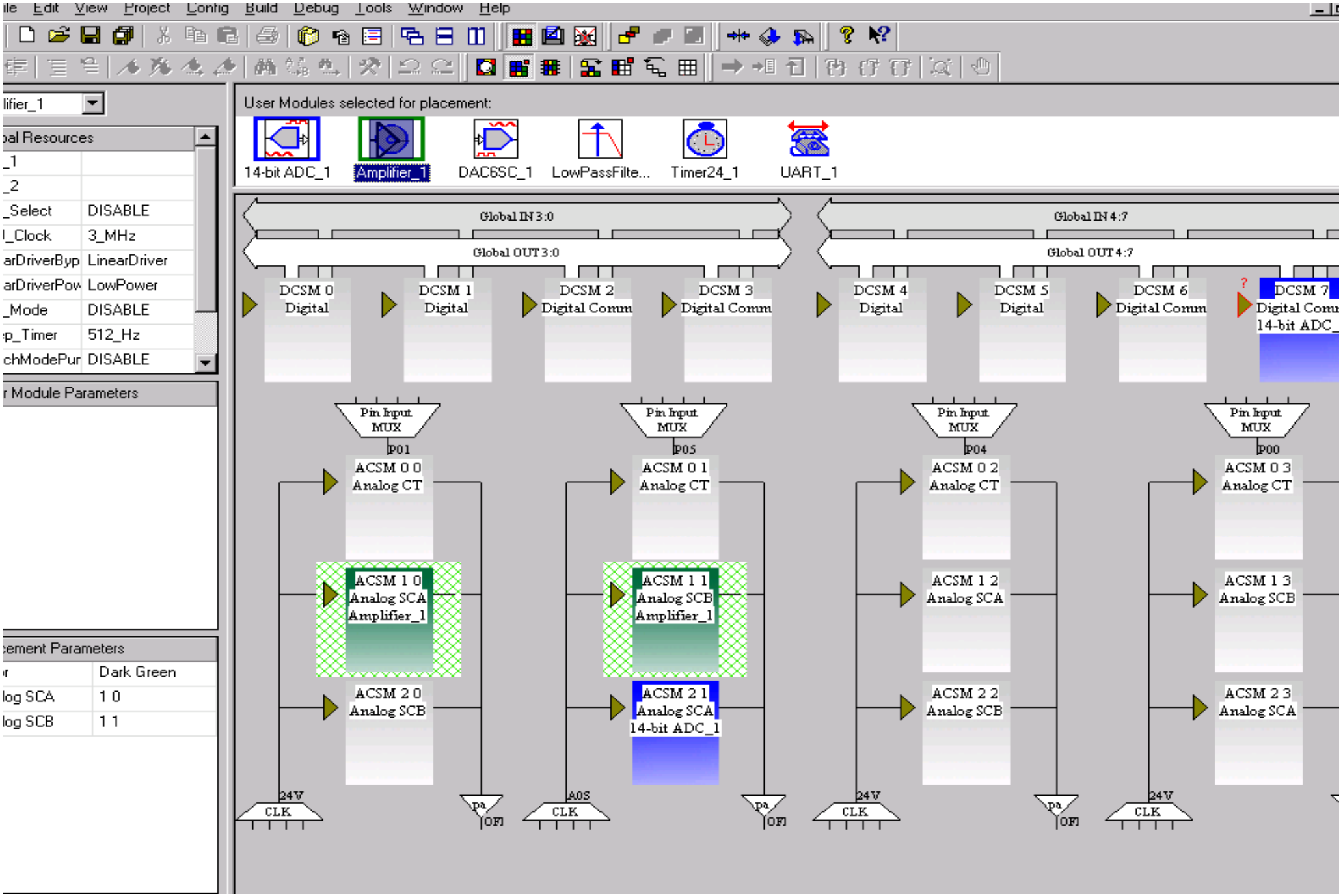


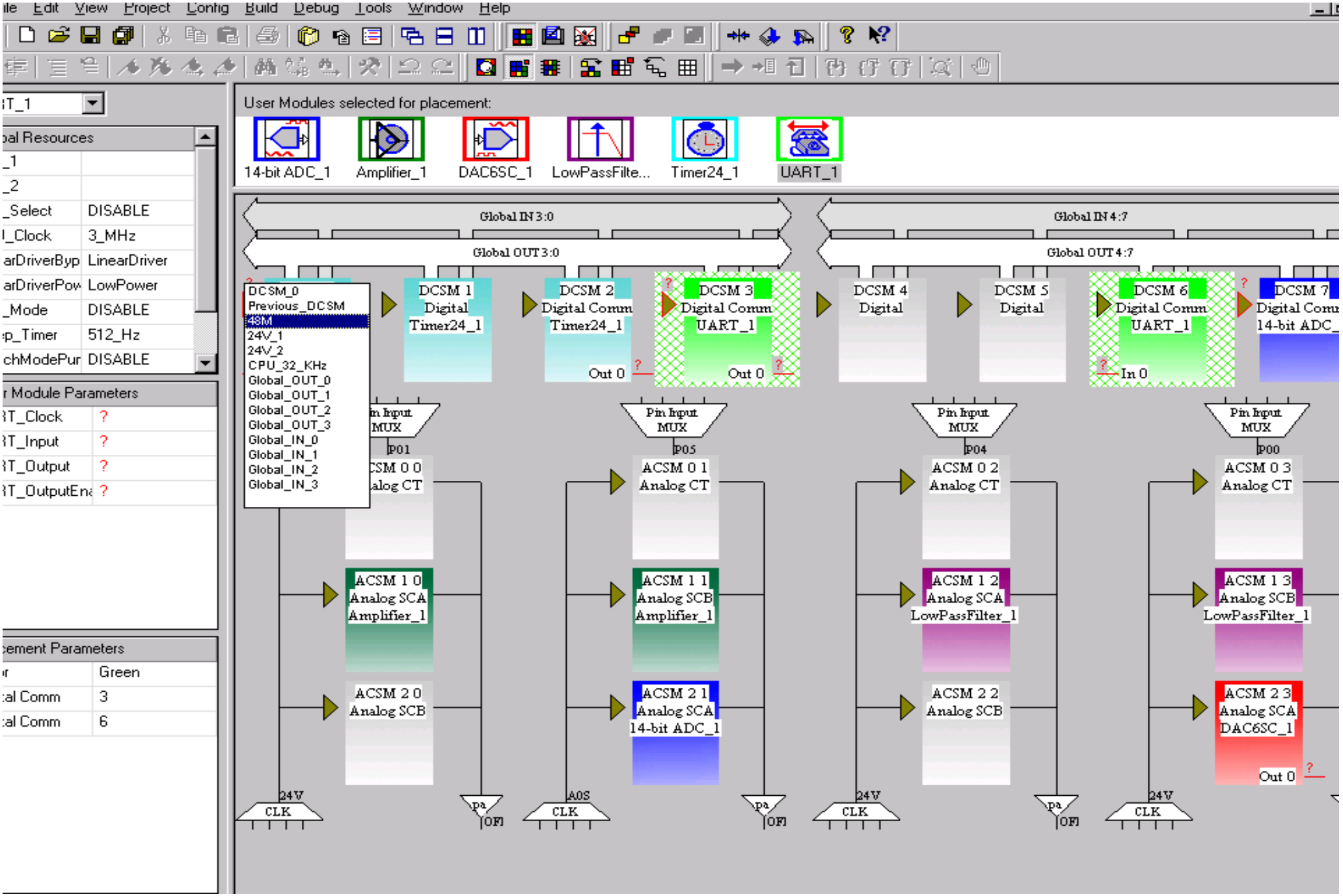
ile Edit View Project Config Build Debug Tools Window Help
Timers
Timer8
Timer32
Timer8
Timer16
Timer24
Counters
PWMs
rial User Modules
PRSs
ADCs
Filters
Amplifiers
DACs
User Modules selected for placement:
Timer24_1
Internal 8-Bit Data Bus
RAM
Data Registers
RAM
RAM
Period
DR1
Auto-
Reload
Time
DR0
Compare
CaptureVal
DR2
Timer Clock
from Clock Select Logic
Output may be
Configured to Drive a Pin
or SoCbloc Input
Configurable
IntReq
on Capture
Output
Total
Used
Analog Blocks 12 0
Digital Blocks 8 3
RAM 256 2
ROM 16384 100
24-bit down timer with period and capture registers
Timer_24
Resources: Required Optional
SoCBlocs 3 Digital, 0 Analog
Memory TBD FLASH, TBD SRAM
Pins 1 per external I/O and clock
Other Modules
Resources
Overview
Diagram
Features
Description
Specs
Options
API

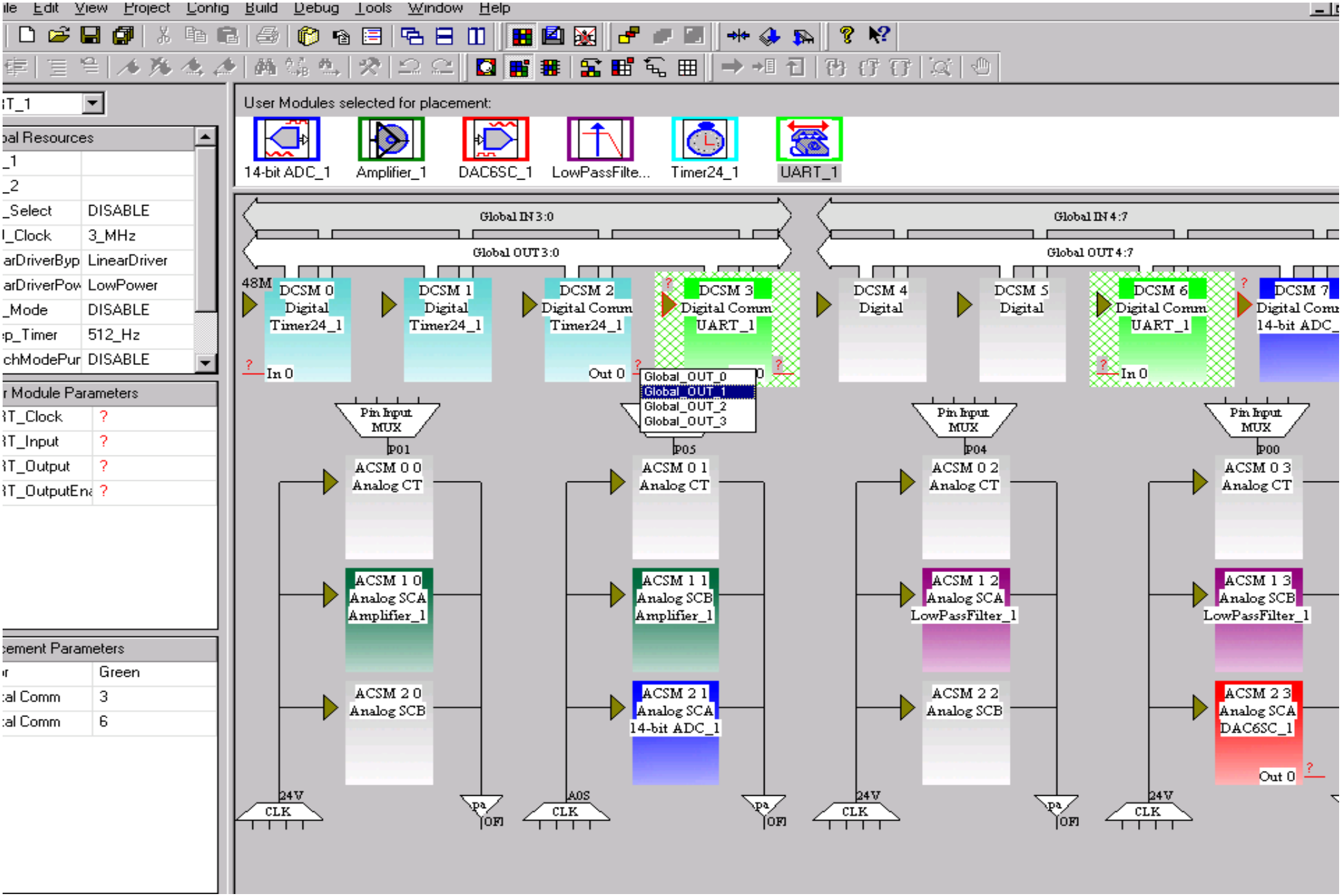
File Edit View Project Config Build Debug Tools Window Help
Timers
Counters
PWMs
rial User Modules
Transmit8
Receive8
SPIM
SPIS
CRC16
UART
PRSs
ADCs
Filters
Amplifiers
DACs
User Modules selected for placement:
Timer24_1
UART_1
Internal 8-bit Data Bus
TX Data Registers
TX Buffer
TX:DR1
Transmitter Shift Register
TX:DR0
Configurable bit Reg on TX Buffer Empty
TX Output maybe Configured to Drive a Pin or SoCbloc Input
Transmitter Clock from Clock Select Logic (must be 8x desired TX rate)
Internal 8-bit Data Bus
RX Data Registers
Serial Receive from External Pin or internal SoCbloc
Receive Shift Register
RX:DR0
RX Buffer
RX:DR1
Configurable bit Reg on RX Buffer Full
Receiver Clock from Clock Select Logic (must be 8x desired RX rate)
Total
Used
Analog Blocks 12 0
Digital Blocks 8 5
RAM 256 4
ROM 16384 200
Universal Asynchronous Receiver/Transmitter
UART
Resources: Required Optional
SoCBlocs 2 Digital, 0 Analog
Memory TBD FLASH, TBD SRAM
Pins 1 per external I/O and clock
Other Modules Baud Generator, CRC
Resources Overview Diagram Features Description Specs Options API

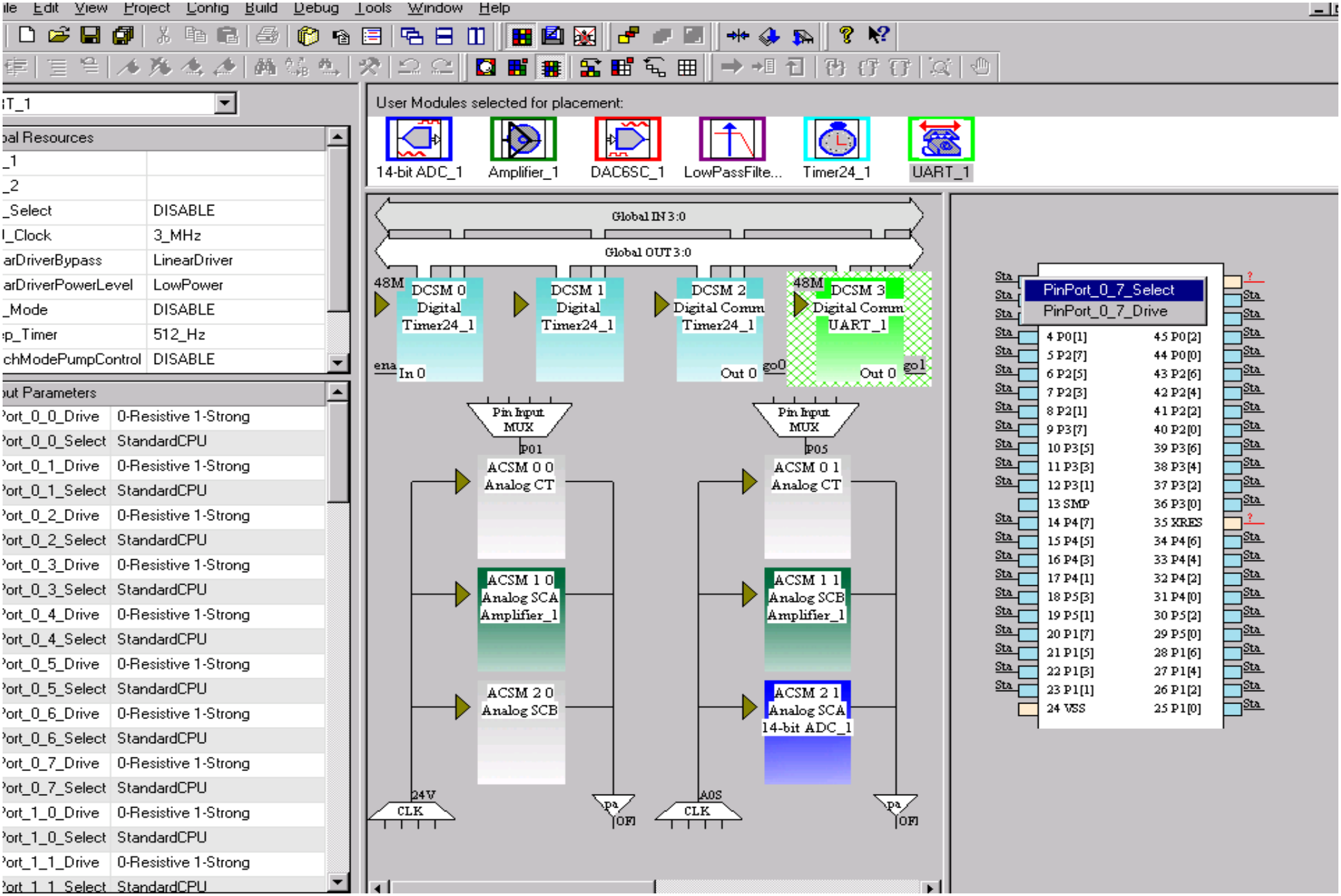

ile Edit View Project Config Build Debug Tools Window Help
Timers
Counters
PWMs
rial User Modules
PRSs
ADCs
GenericADC
14-bit ADC
12-bit ADC
10-bit ADC
Filters
Amplifiers
DACs
User Modules selected for placement:
Timer24_1
UART_1
14-bit ADC_1
bit clock
Timer
word clock
(interrupt)
+Vref
-Vref
Vin
Counter
Result on
data bus
Total
Used
Analog Blocks
12
1
Digital Blocks
8
6
RAM
256
6
ROM
16384
300
14-Bit Incremental ADC, DEMO ONLY
ADC
Resources:
Required
Optional
SoCblocs
0 Digital, 2 Analog
Memory
TBD FLASH, TBD SRAM
Pins
1 per external I/O and clock
Other Modules
Asdfjasdfjadf;lasdfl;asdfadjfdjfas;
DAC11SC
Resources
Overview
Diagram
Features
Description

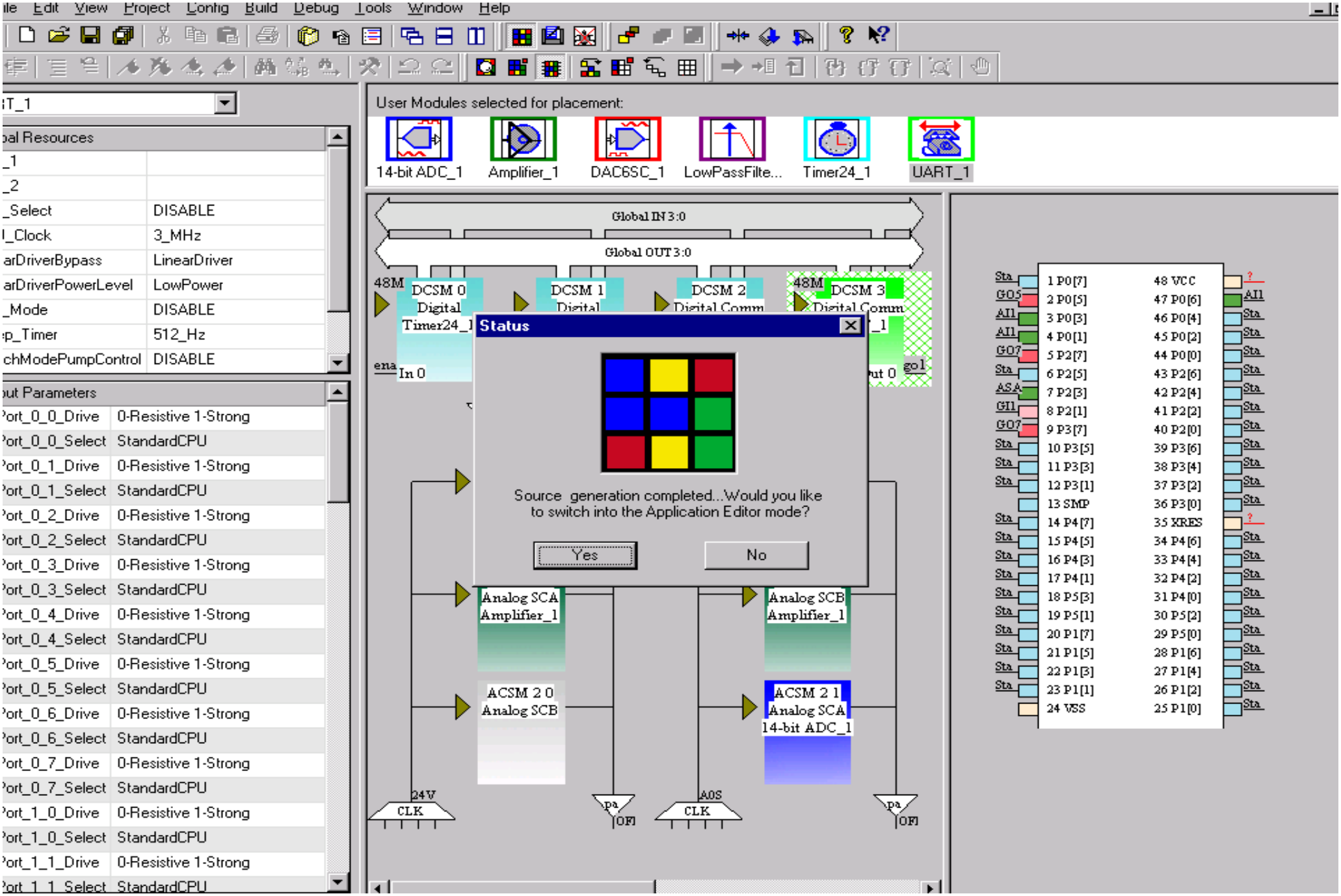

Edit View Project Config Build Debug Tools Window Help
Next Position
User Modules selected for placement:
14-bit ADC_1
Amplifier_1
DAC6SC_1
LowPassFilte...
Timer24_1
UART_1
Global IN 3:0
Global OUT 3:0
Global IN 4:7
Global OUT 4:7
DCSM 0 Digital
DCSM 1 Digital
DCSM 2 Digital Comm
DCSM 3 Digital Comm
DCSM 4 Digital
DCSM 5 Digital
DCSM 6 Digital Comm
DCSM 7 Digital Comm
Pin Input MUX
P01
P05
P04
P00
ACSM 0 0 Analog CT
ACSM 1 0 Analog SCA
ACSM 2 0 Analog SCB
ACSM 0 1 Analog CT
ACSM 1 1 Analog SCB
ACSM 2 1 Analog SCA
ACSM 0 2 Analog CT
ACSM 1 2 Analog SCA
ACSM 2 2 Analog SCB
ACSM 0 3 Analog CT
ACSM 1 3 Analog SCB
ACSM 2 3 Analog SCA
24V
CLK
Global Resources
Module Parameters
Placement Parameters

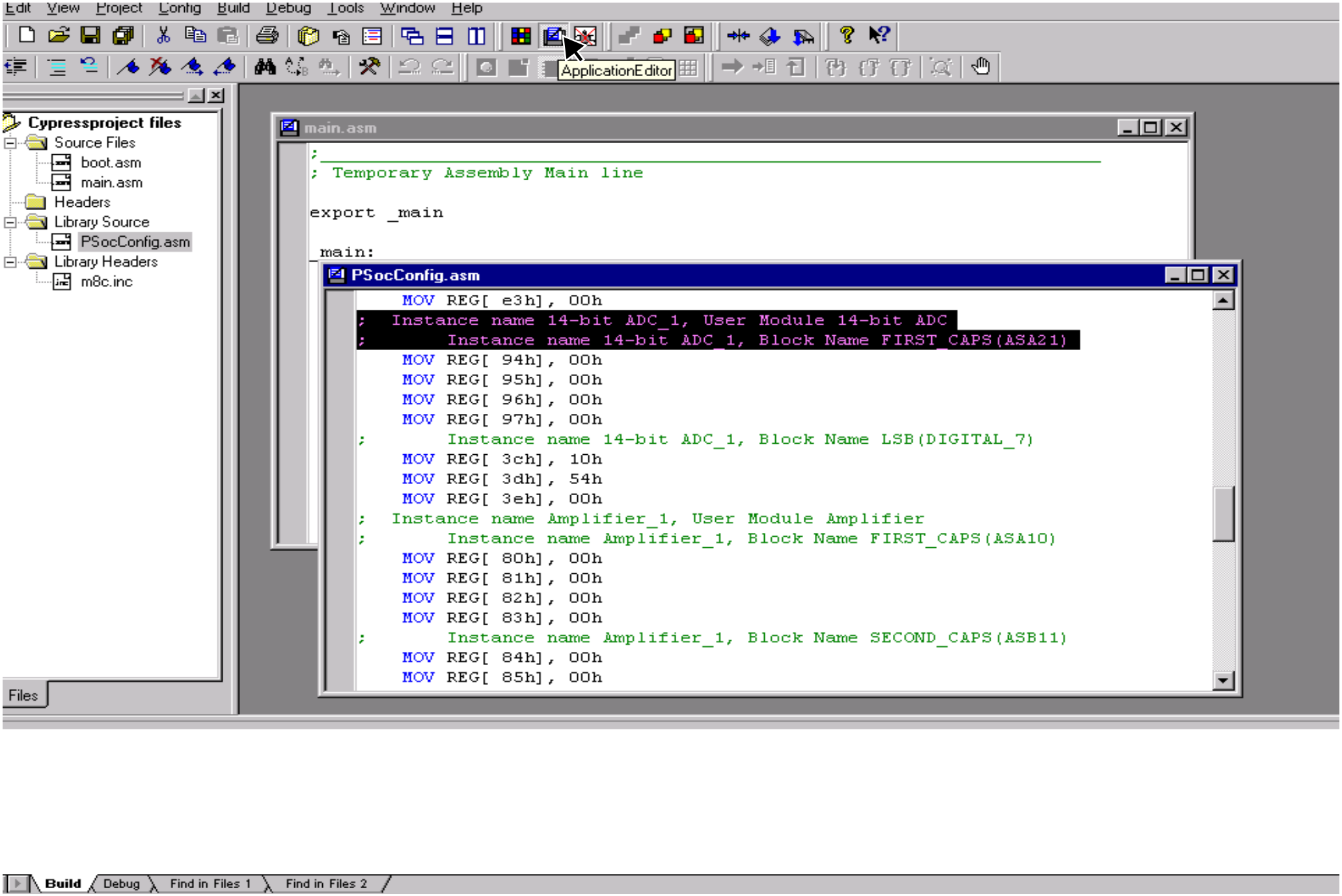

Edit View Project Config Build Debug Tools Window Help
lifier_1
bal Resources
_1
_2
_Select DISABLE
l_Clock 3_MHz
arDriverByp LinearDriver
arDriverPow LowPower
_Mode DISABLE
p_Timer 512_Hz
chModePur DISABLE
r Module Parameters
cement Parameters
r Dark Green
log SCA 1 0
log SCB 1 1
User Modules selected for placement:
14-bit ADC_1
Amplifier_1
DAC6SC_1
LowPassFilte...
Timer24_1
UART_1
Global IN 3:0
Global OUT 3:0
Global IN 4:7
Global OUT 4:7
DCSM 0 Digital
DCSM 1 Digital
DCSM 2 Digital Comm
DCSM 3 Digital Comm
DCSM 4 Digital
DCSM 5 Digital
DCSM 6 Digital Comm
DCSM 7 Digital Comm
14-bit ADC_
Pin Input MUX
P01
P05
P04
P00
ACSM 0 0 Analog CT
ACSM 0 1 Analog CT
ACSM 0 2 Analog CT
ACSM 0 3 Analog CT
ACSM 1 0 Analog SCA Amplifier_1
ACSM 1 1 Analog SCB Amplifier_1
ACSM 1 2 Analog SCA
ACSM 1 3 Analog SCB
ACSM 2 0 Analog SCB
ACSM 2 1 Analog SCA 14-bit ADC_1
ACSM 2 2 Analog SCB
ACSM 2 3 Analog SCA
24V
CLK
A0S
pa
OFI


Edit View Project Config Build Debug Tools Window Help
User Modules selected for placement:
14-bit ADC_1
Amplifier_1
DAC6SC_1
LowPassFilte...
Timer24_1
UART_1
Global IN 3:0
Global OUT 3:0
Global IN 4:7
Global OUT 4:7
DCSM_0
Previous_DCSM
48M
24V_1
24V_2
CPU_32_KHz
Global_OUT_0
Global_OUT_1
Global_OUT_2
Global_OUT_3
Global_IN_0
Global_IN_1
Global_IN_2
Global_IN_3
DCSM 1
Digital
Timer24_1
DCSM 2
Digital Comm
Timer24_1
Out 0
DCSM 3
Digital Comm
UART_1
Out 0
DCSM 4
Digital
DCSM 5
Digital
DCSM 6
Digital Comm
UART_1
In 0
DCSM 7
Digital Comm
14-bit ADC_
Pin Input
MUX
P01
P05
P04
P00
ACSM 0 1
Analog CT
ACSM 0 2
Analog CT
ACSM 0 3
Analog CT
ACSM 1 0
Analog SCA
Amplifier_1
ACSM 1 1
Analog SCB
Amplifier_1
ACSM 1 2
Analog SCA
LowPassFilter_1
ACSM 1 3
Analog SCB
LowPassFilter_1
ACSM 2 0
Analog SCB
ACSM 2 1
Analog SCA
14-bit ADC_1
ACSM 2 2
Analog SCB
ACSM 2 3
Analog SCA
DAC6SC_1
Out 0
24V
CLK
A0S
CLK
24V
CLK
24V
CLK
Global Resources
_Select DISABLE
_Clock 3_MHz
arDriverByp LinearDriver
arDriverPow LowPower
_Mode DISABLE
p_Timer 512_Hz
chModePur DISABLE
Module Parameters
T_Clock ?
T_Input ?
T_Output ?
T_OutputEna ?
Green
al Comm 3
al Comm 6

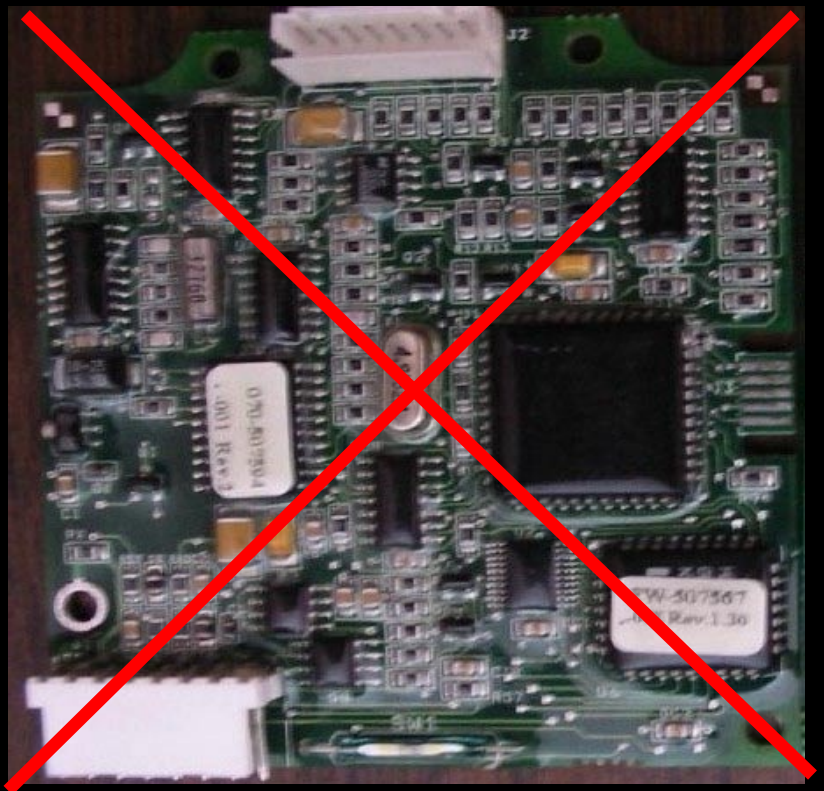

Edit View Project Config Build Debug Tools Window Help
User Modules selected for placement:
14-bit ADC_1
Amplifier_1
DAC6SC_1
LowPassFilte...
Timer24_1
UART_1
Global IN 3:0
Global OUT 3:0
Global IN 4:7
Global OUT 4:7
48M
DCSM 0 Digital Timer24_1
DCSM 1 Digital Timer24_1
DCSM 2 Digital Comm Timer24_1
DCSM 3 Digital Comm UART_1
DCSM 4 Digital
DCSM 5 Digital
DCSM 6 Digital Comm UART_1
DCSM 7 Digital Comm 14-bit ADC_
In 0
Out 0
Global_OUT_0
Global_OUT_1
Global_OUT_2
Global_OUT_3
Pin Input MUX
P01
P05
P04
P00
ACSM 0 0 Analog CT
ACSM 0 1 Analog CT
ACSM 0 2 Analog CT
ACSM 0 3 Analog CT
ACSM 1 0 Analog SCA Amplifier_1
ACSM 1 1 Analog SCB Amplifier_1
ACSM 1 2 Analog SCA LowPassFilter_1
ACSM 1 3 Analog SCB LowPassFilter_1
ACSM 2 0 Analog SCB
ACSM 2 1 Analog SCA 14-bit ADC_1
ACSM 2 2 Analog SCB
ACSM 2 3 Analog SCA DAC6SC_1
Out 0
24V
CLK
Global Resources
_Select DISABLE
_Clock 3_MHz
arDriverByp LinearDriver
arDriverPow LowPower
_Mode DISABLE
p_Timer 512_Hz
chModePur DISABLE
Module Parameters
T_Clock ?
T_Input ?
T_Output ?
T_OutputEna ?
Green
al Comm 3
al Comm 6


Edit View Project Config Build Debug Tools Window Help
User Modules selected for placement:
14-bit ADC_1
Amplifier_1
DAC6SC_1
LowPassFilte...
Timer24_1
UART_1
Global IN 3:0
Global OUT 3:0
48M
DCSM 0
Digital
Timer24_1
DCSM 1
Digital
Timer24_1
DCSM 2
Digital Comm
Timer24_1
48M
DCSM 3
Digital Comm
UART_1
ena
In 0
Out 0
go0
Out 0
go1
Pin Input
MUX
P01
Pin Input
MUX
P05
ACSM 0 0
Analog CT
ACSM 0 1
Analog CT
ACSM 1 0
Analog SCA
Amplifier_1
ACSM 1 1
Analog SCB
Amplifier_1
ACSM 2 0
Analog SCB
ACSM 2 1
Analog SCA
14-bit ADC_1
24V
CLK
pa
OFI
A0S
CLK
pa
OFI
PinPort_0_7_Select
PinPort_0_7_Drive
4 P0[1]
5 P2[7]
6 P2[5]
7 P2[3]
8 P2[1]
9 P3[7]
10 P3[5]
11 P3[3]
12 P3[1]
13 SMP
14 P4[7]
15 P4[5]
16 P4[3]
17 P4[1]
18 P5[3]
19 P5[1]
20 P1[7]
21 P1[5]
22 P1[3]
23 P1[1]
24 VSS
45 P0[2]
44 P0[0]
43 P2[6]
42 P2[4]
41 P2[2]
40 P2[0]
39 P3[6]
38 P3[4]
37 P3[2]
36 P3[0]
35 XRES
34 P4[6]
33 P4[4]
32 P4[2]
31 P4[0]
30 P5[2]
29 P5[0]
28 P1[6]
27 P1[4]
26 P1[2]
25 P1[0]
Sta
_Select DISABLE
_Clock 3_MHz
arDriverBypass LinearDriver
arDriverPowerLevel LowPower
_Mode DISABLE
p_Timer 512_Hz
chModePumpControl DISABLE
Port_0_0_Drive 0-Resistive 1-Strong
Port_0_0_Select StandardCPU
Port_0_1_Drive 0-Resistive 1-Strong
Port_0_1_Select StandardCPU
Port_0_2_Drive 0-Resistive 1-Strong
Port_0_2_Select StandardCPU
Port_0_3_Drive 0-Resistive 1-Strong
Port_0_3_Select StandardCPU
Port_0_4_Drive 0-Resistive 1-Strong
Port_0_4_Select StandardCPU
Port_0_5_Drive 0-Resistive 1-Strong
Port_0_5_Select StandardCPU
Port_0_6_Drive 0-Resistive 1-Strong
Port_0_6_Select StandardCPU
Port_0_7_Drive 0-Resistive 1-Strong
Port_0_7_Select StandardCPU
Port_1_0_Drive 0-Resistive 1-Strong
Port_1_0_Select StandardCPU
Port_1_1_Drive 0-Resistive 1-Strong
Port_1_1_Select StandardCPU

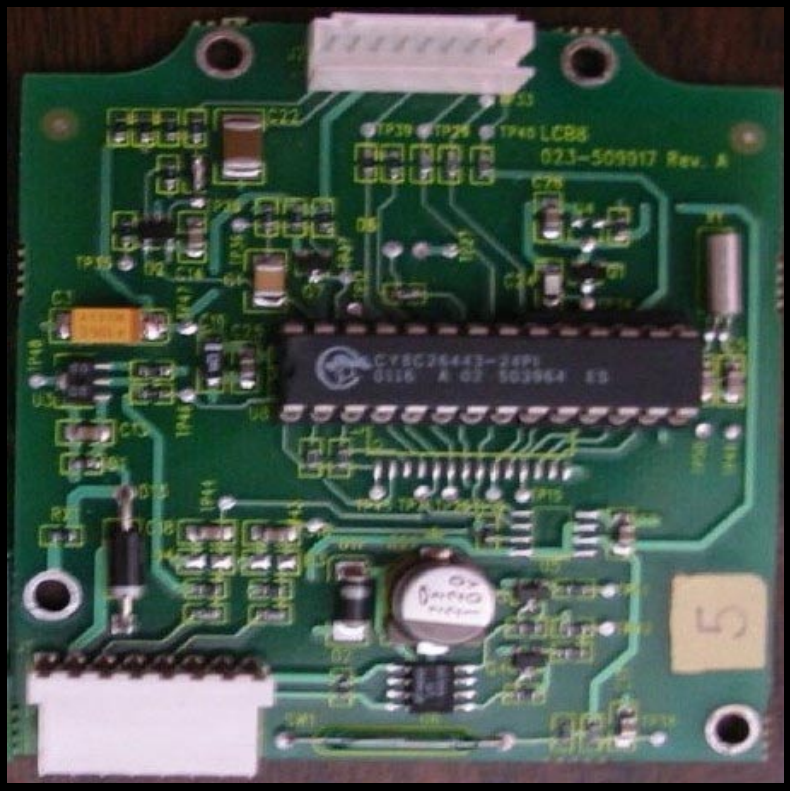

Edit View Project Config Build Debug Tools Window Help
User Modules selected for placement:
14-bit ADC_1
Amplifier_1
DAC6SC_1
LowPassFilte...
Timer24_1
UART_1
Global IN 3:0
Global OUT 3:0
DCSM 0
DCSM 1
DCSM 2
DCSM 3
Status
Source generation completed...Would you like to switch into the Application Editor mode?
Yes
No
Analog SCA Amplifier_1
Analog SCB Amplifier_1
ACSM 2 0 Analog SCB
ACSM 2 1 Analog SCA 14-bit ADC_1
1 P0[7]
2 P0[5]
3 P0[3]
4 P0[1]
5 P2[7]
6 P2[5]
7 P2[3]
8 P2[1]
9 P3[7]
10 P3[5]
11 P3[3]
12 P3[1]
13 SMP
14 P4[7]
15 P4[5]
16 P4[3]
17 P4[1]
18 P5[3]
19 P5[1]
20 P1[7]
21 P1[5]
22 P1[3]
23 P1[1]
24 VSS
48 VCC
47 P0[6]
46 P0[4]
45 P0[2]
44 P0[0]
43 P2[6]
42 P2[4]
41 P2[2]
40 P2[0]
39 P3[6]
38 P3[4]
37 P3[2]
36 P3[0]
35 XRES
34 P4[6]
33 P4[4]
32 P4[2]
31 P4[0]
30 P5[2]
29 P5[0]
28 P1[6]
27 P1[4]
26 P1[2]
25 P1[0]


Edit View Project Config Build Debug Tools Window Help
ApplicationEditor
Cypressproject files
Source Files
boot.asm
main.asm
Headers
Library Source
PSocConfig.asm
Library Headers
m8c.inc
Files
main.asm
; Temporary Assembly Main line
export _main
_main:
PSocConfig.asm
MOV REG[e3h], 00h
; Instance name 14-bit ADC_1, User Module 14-bit ADC
; Instance name 14-bit ADC_1, Block Name FIRST_CAPS(ASA21)
MOV REG[94h], 00h
MOV REG[95h], 00h
MOV REG[96h], 00h
MOV REG[97h], 00h
; Instance name 14-bit ADC_1, Block Name LSB(DIGITAL_7)
MOV REG[3ch], 10h
MOV REG[3dh], 54h
MOV REG[3eh], 00h
; Instance name Amplifier_1, User Module Amplifier
; Instance name Amplifier_1, Block Name FIRST_CAPS(ASA10)
MOV REG[80h], 00h
MOV REG[81h], 00h
MOV REG[82h], 00h
MOV REG[83h], 00h
; Instance name Amplifier_1, Block Name SECOND_CAPS(ASB11)
MOV REG[84h], 00h
MOV REG[85h], 00h
Build
Debug
Find in Files 1
Find in Files 2

WHY CHOOSE PSoC?
PARTS REDUCTION



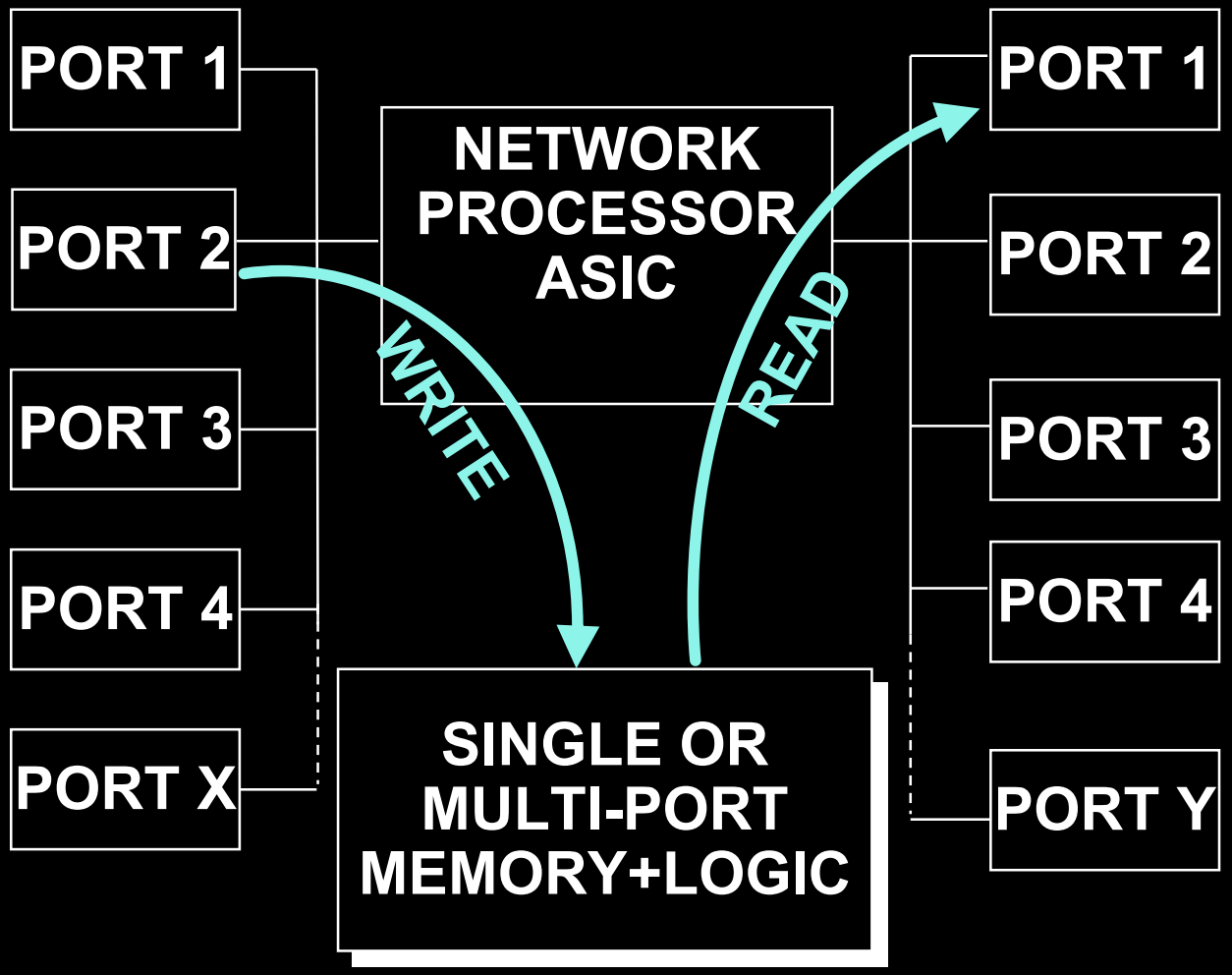
~~90+ Parts~~



20+ Parts

$2.00

MEMORIES IN SWITCHES



CUSTOMER ISSUES

BANDWIDTH

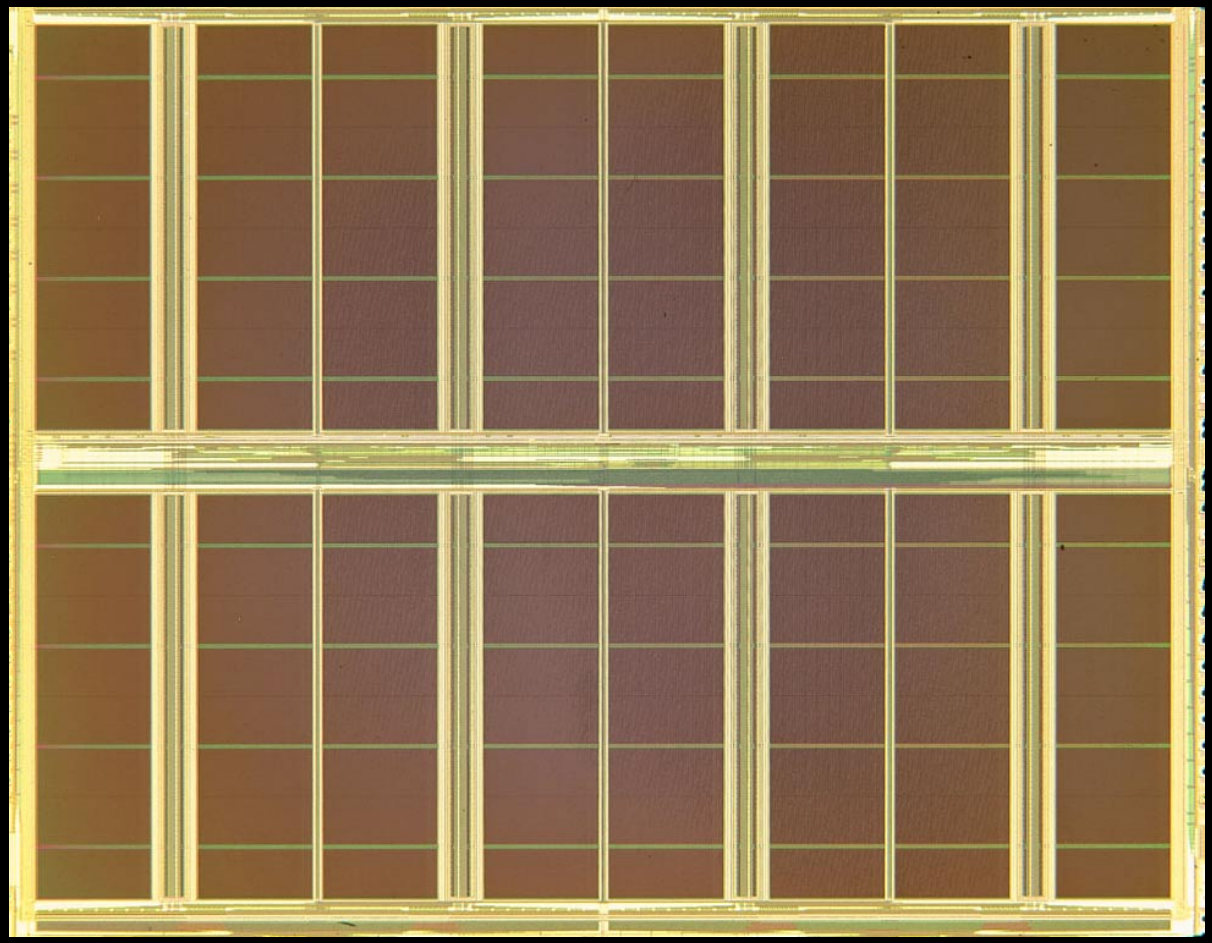
LATENCY

DENSITY

AVAILABILITY

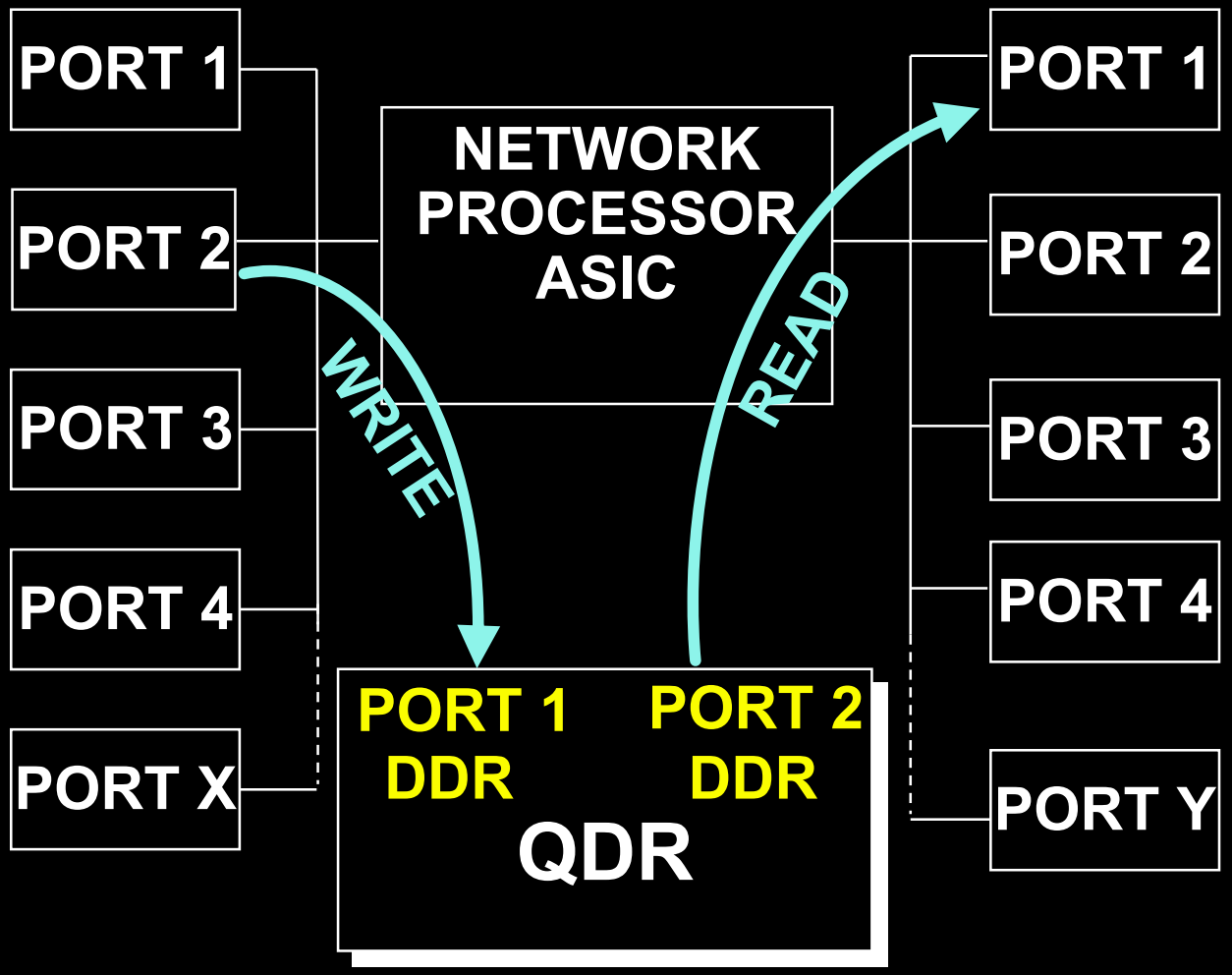
BIT COST

18 M NoBL RAM



PROBLEM: MAKE IT GO FASTER

QUAD DATA RATE (QDR)



CUSTOMER ISSUES

BANDWIDTH

LATENCY

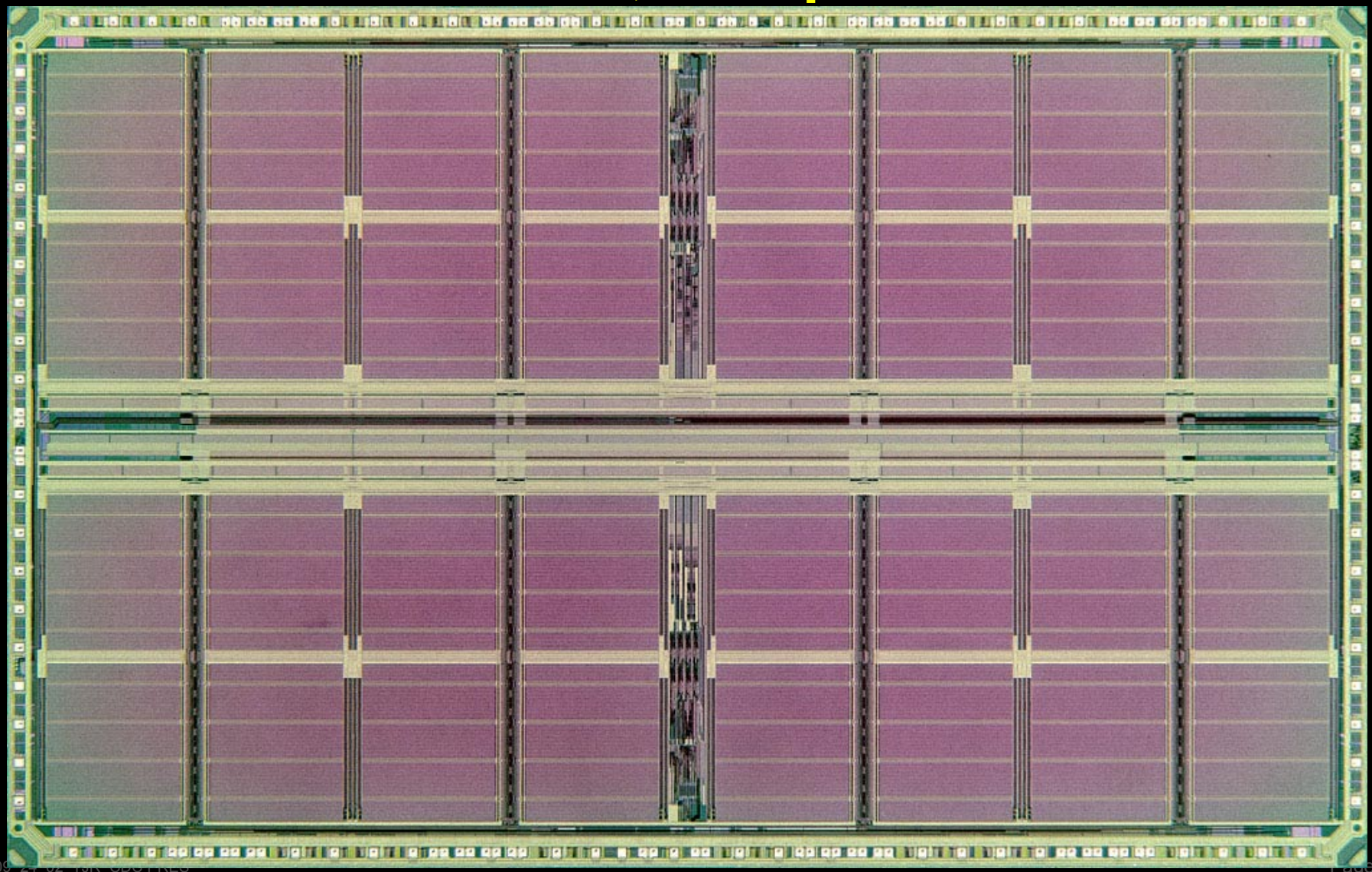
DENSITY

AVAILABILITY

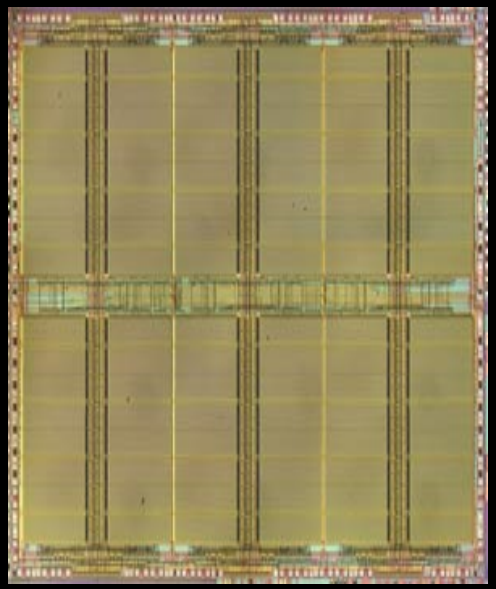
BIT COST

PARTNER: CISCO

QDR, 6 Gbps



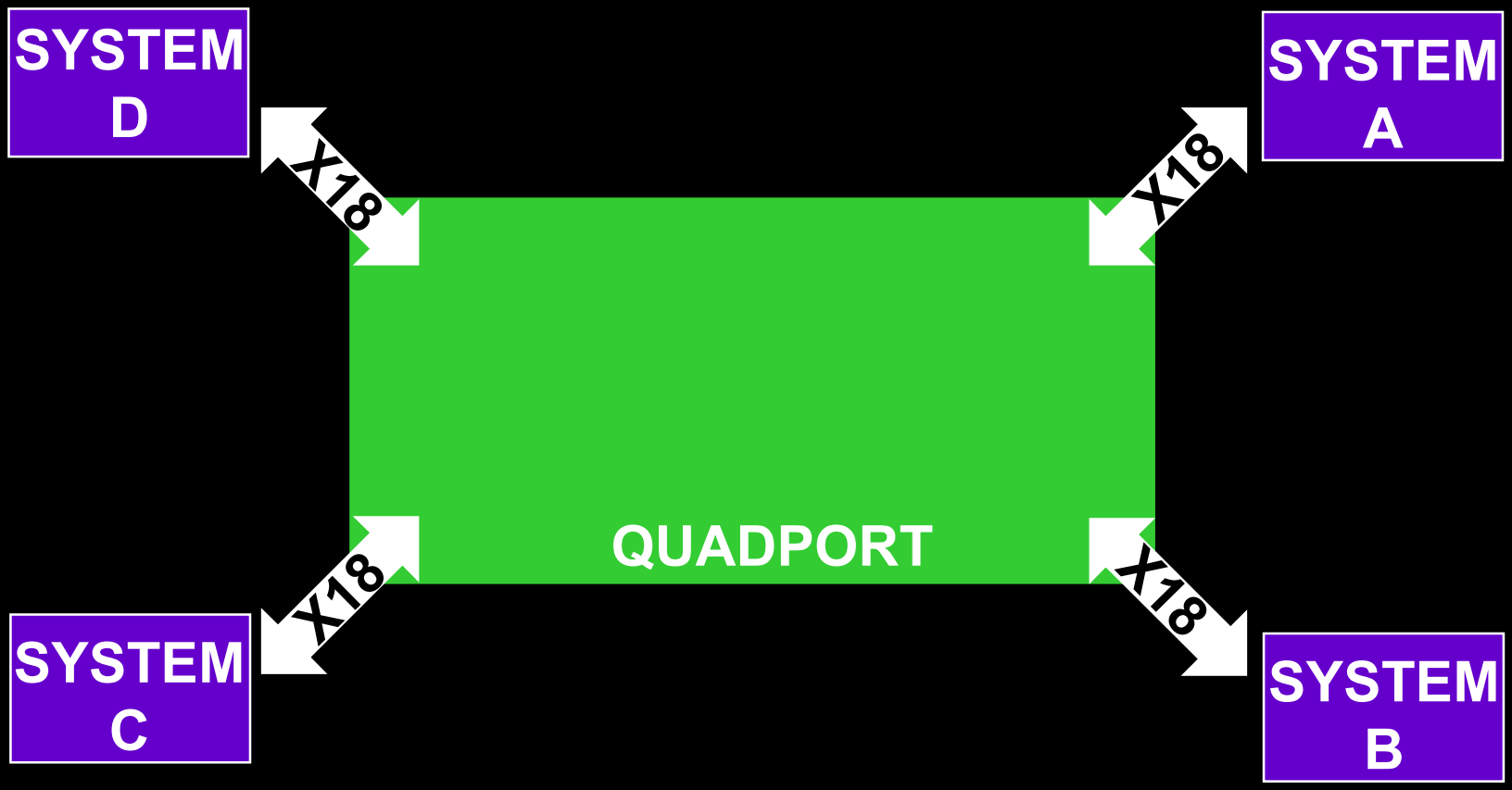
NINE MEGABIT DUAL-PORT RAMs



CYPRESS

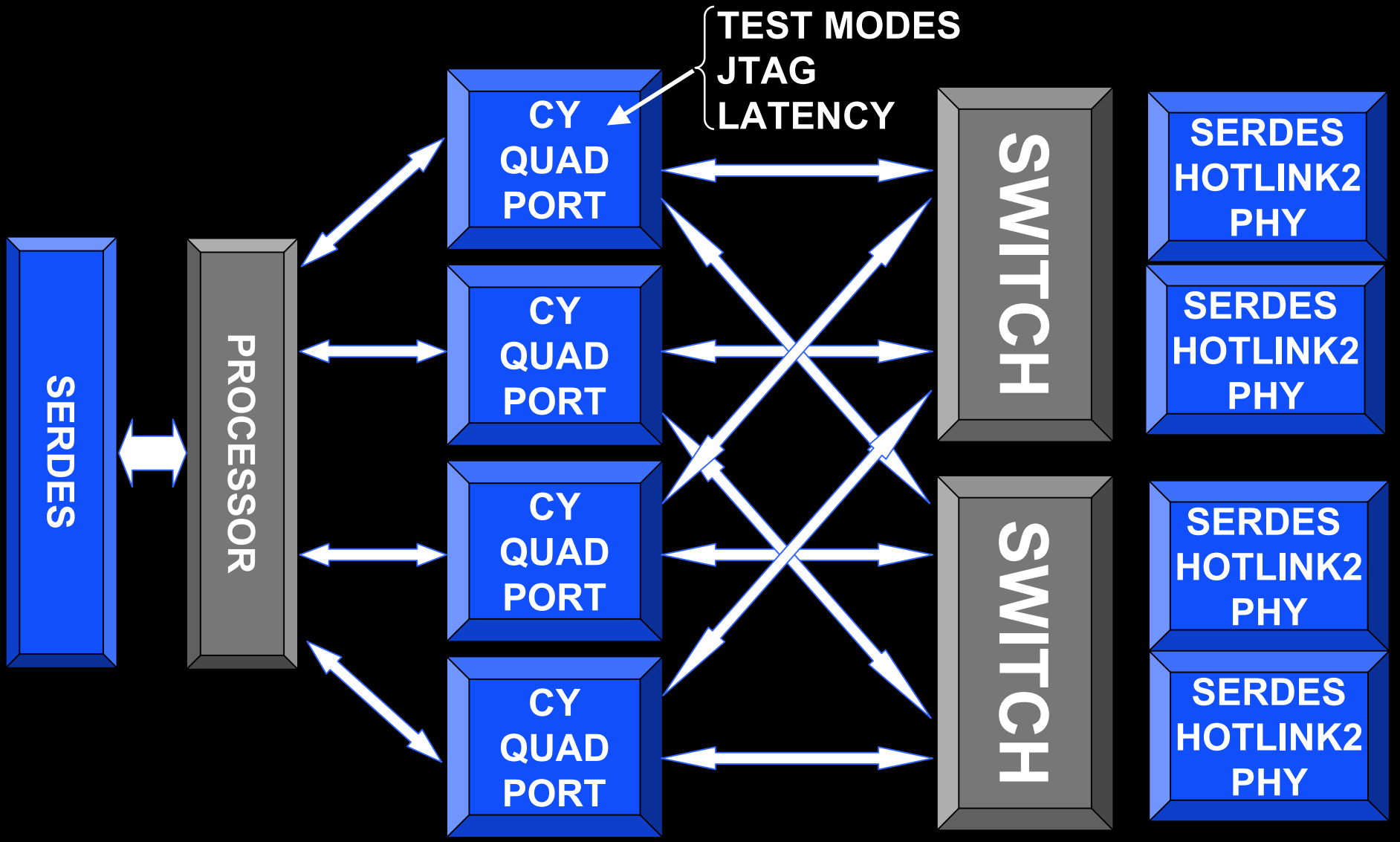
IDT

QUADPORT MEMORY



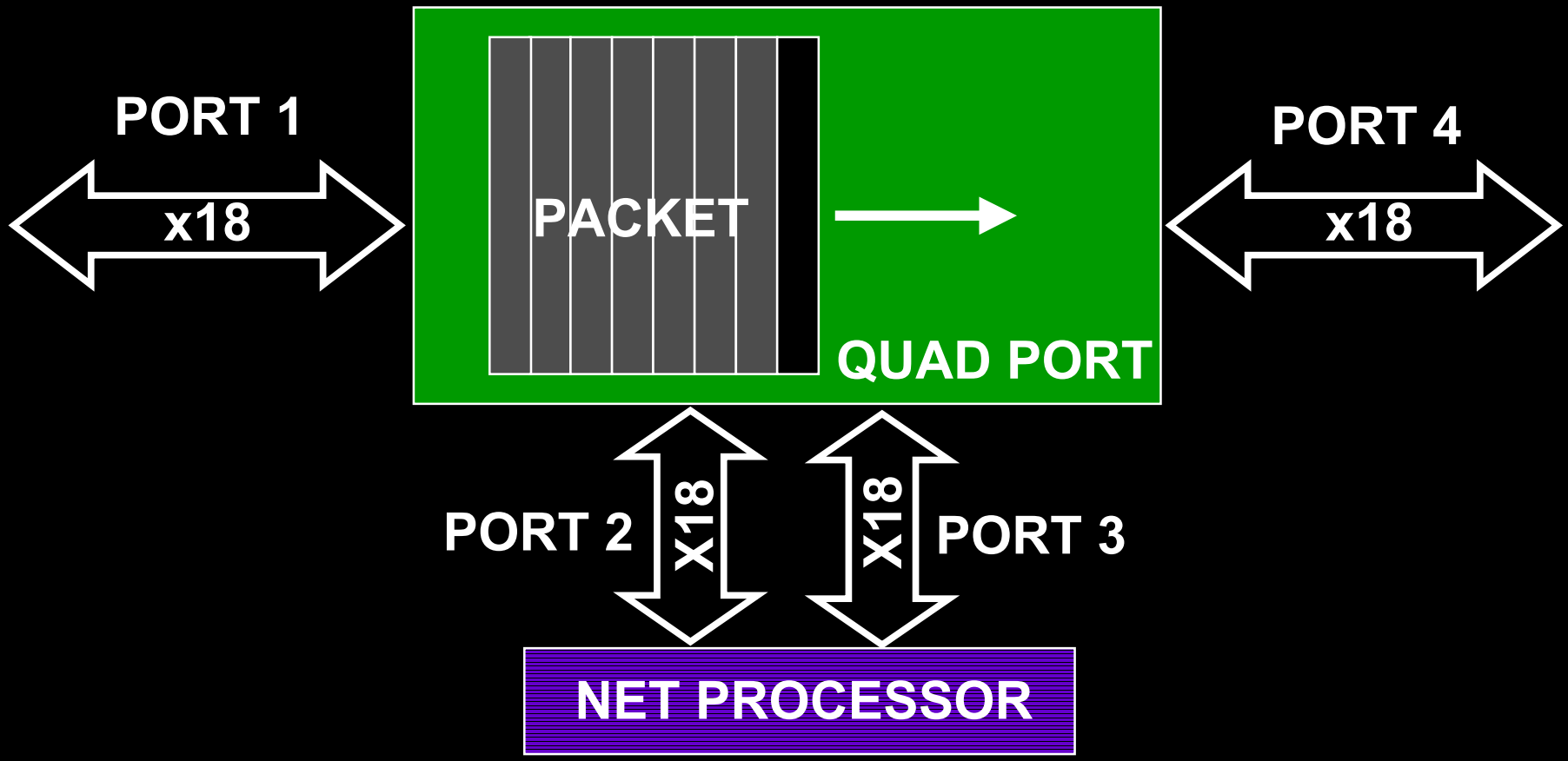
PROBLEM: FAST SWITCHING WITH DATA BUFFERING

RAID DIRECTOR CARD

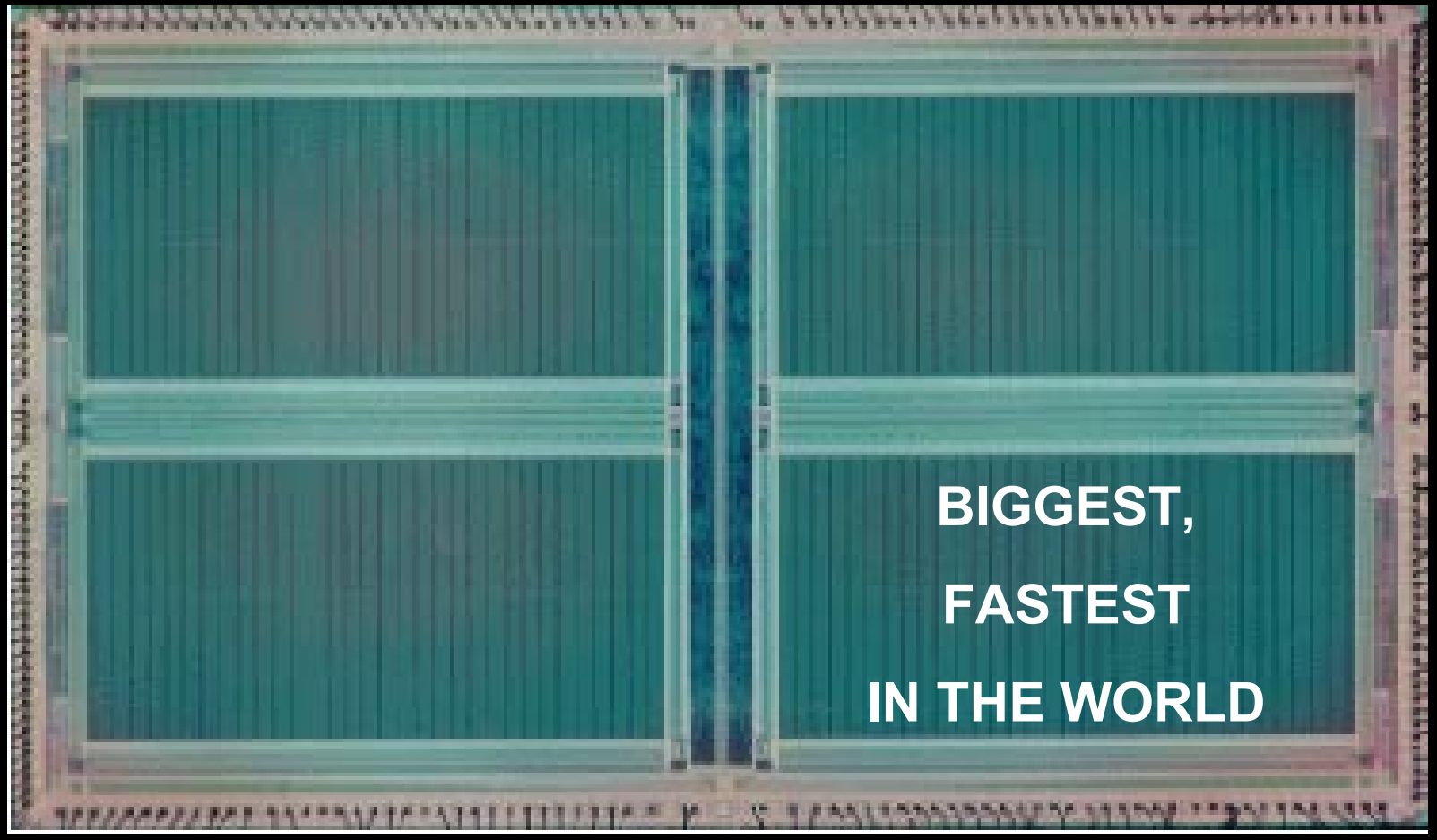


PARTNER: EMC

QUADPORT: PACKET MANIPULATION

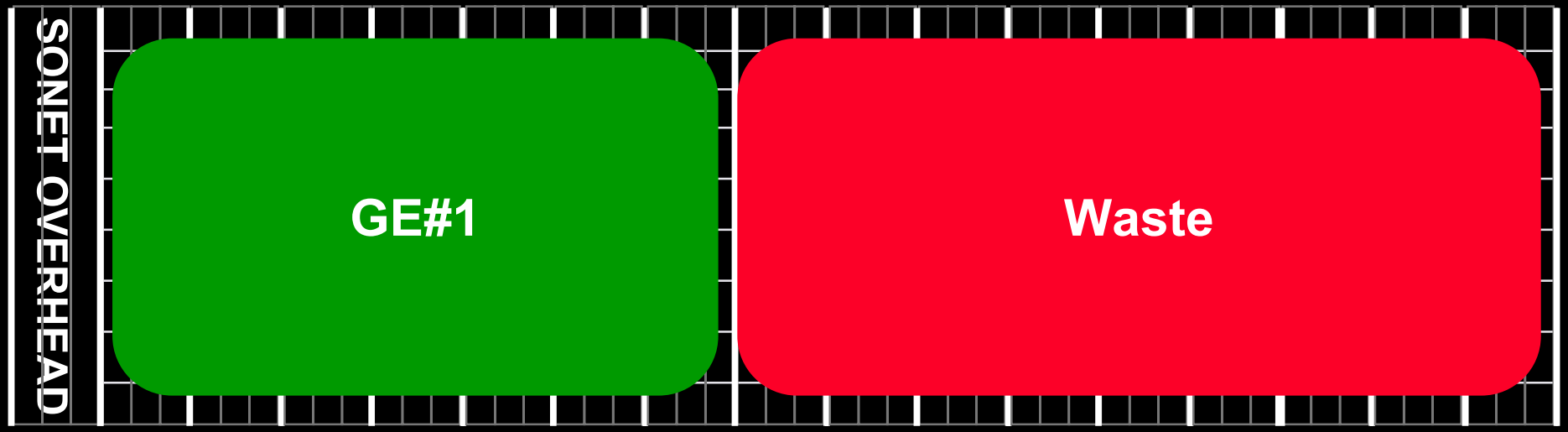


QUAD-PORT, 9.6 GBPS



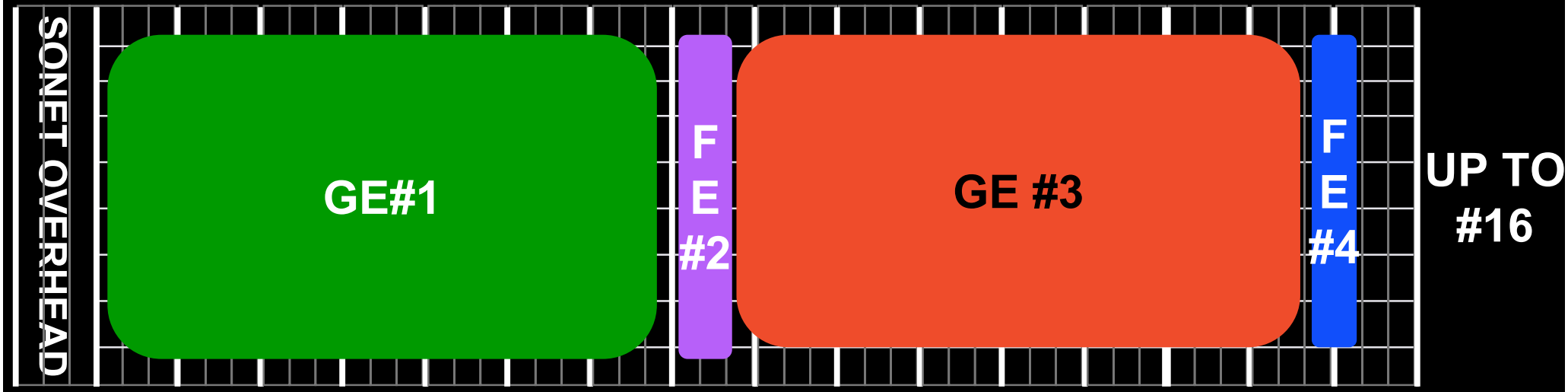
PROBLEM: INEFFICIENCY OF ETHERNET OVER SONET

OC-48 FRAME = 16X STS3 = 48X STS 1



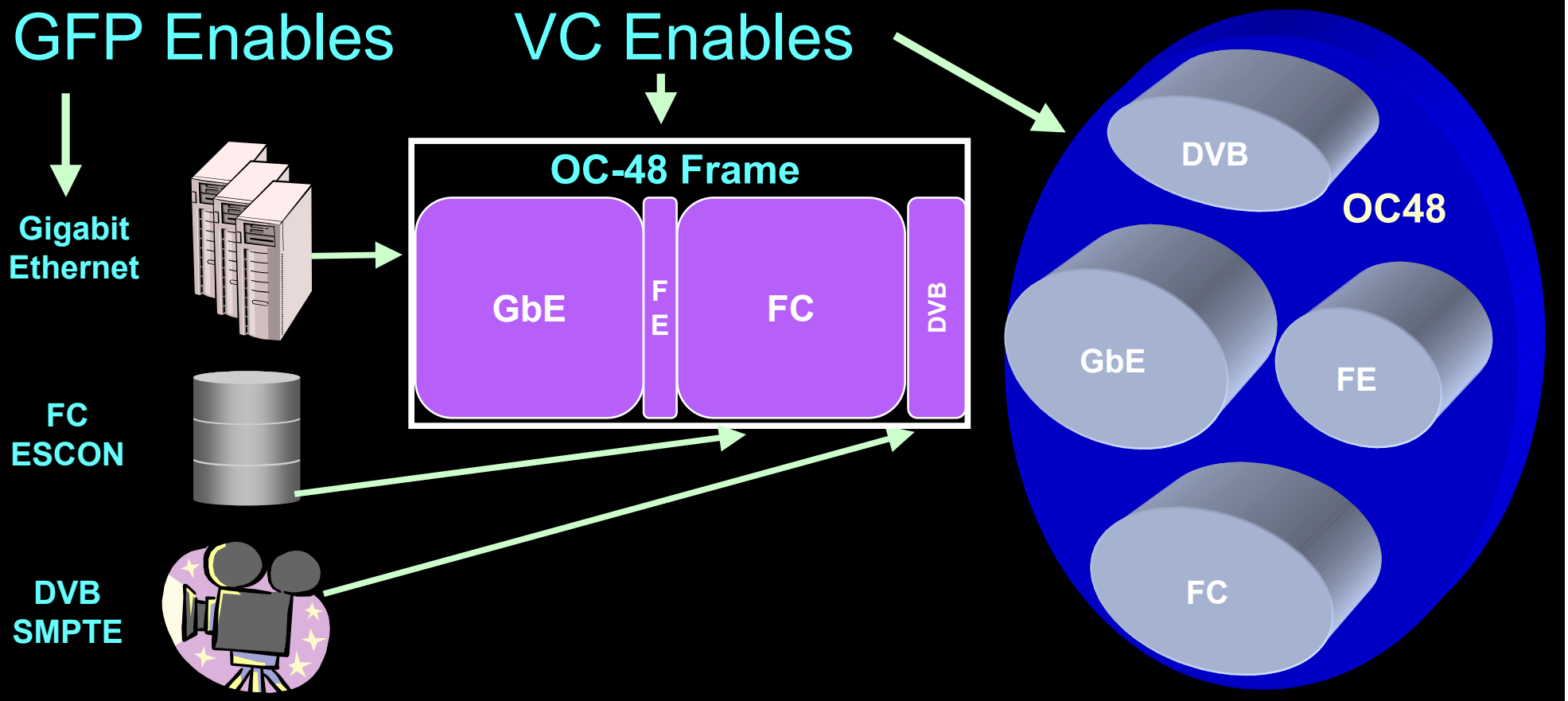
SOLUTION: VIRTUAL CONCATENATION (DYNAMIC BANDWIDTH ALLOCATION)

OC-48 FRAME = 16X STS3 = 48X STS 1



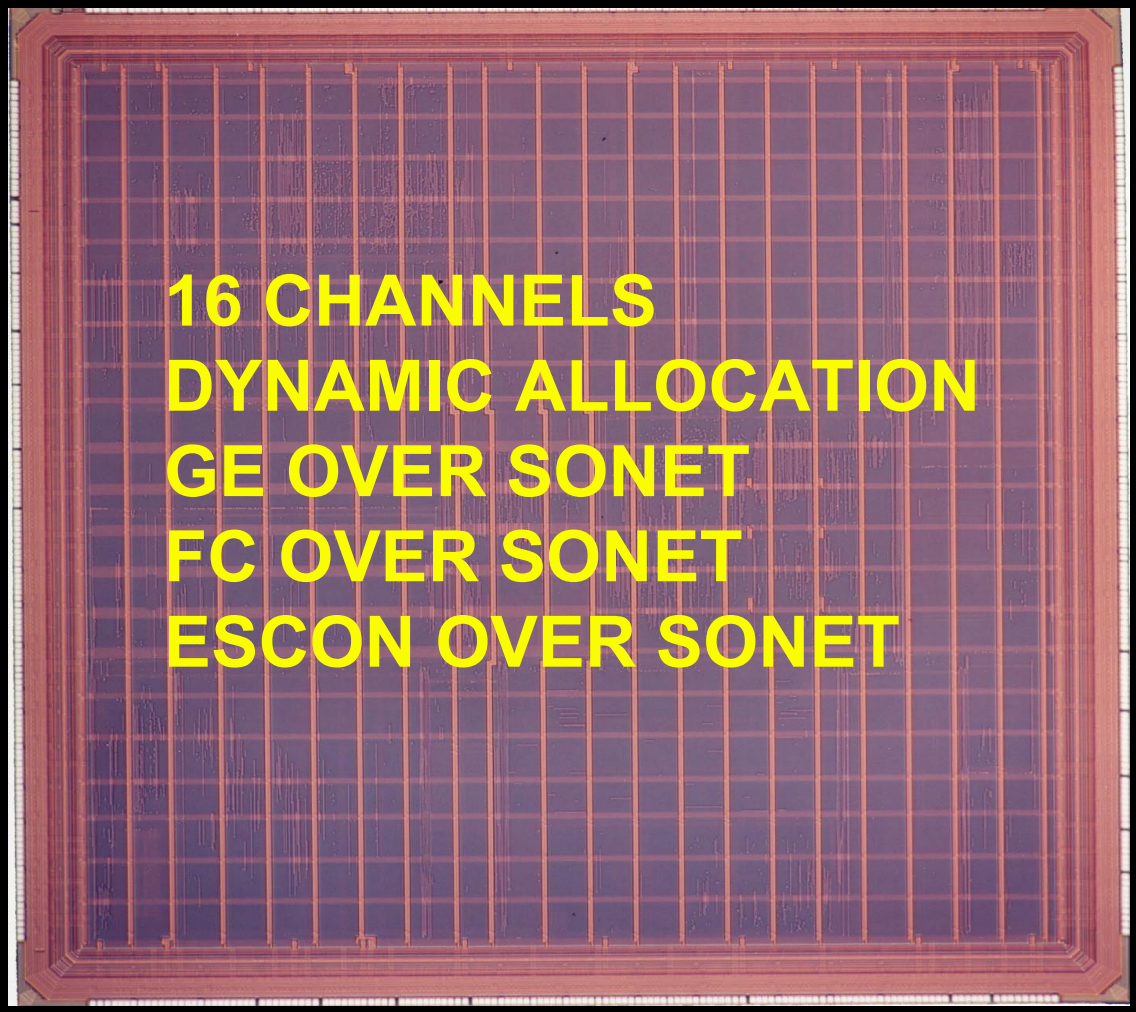
PARTNER: NORTEL

PROBLEM: TOO MANY PROTOCOLS



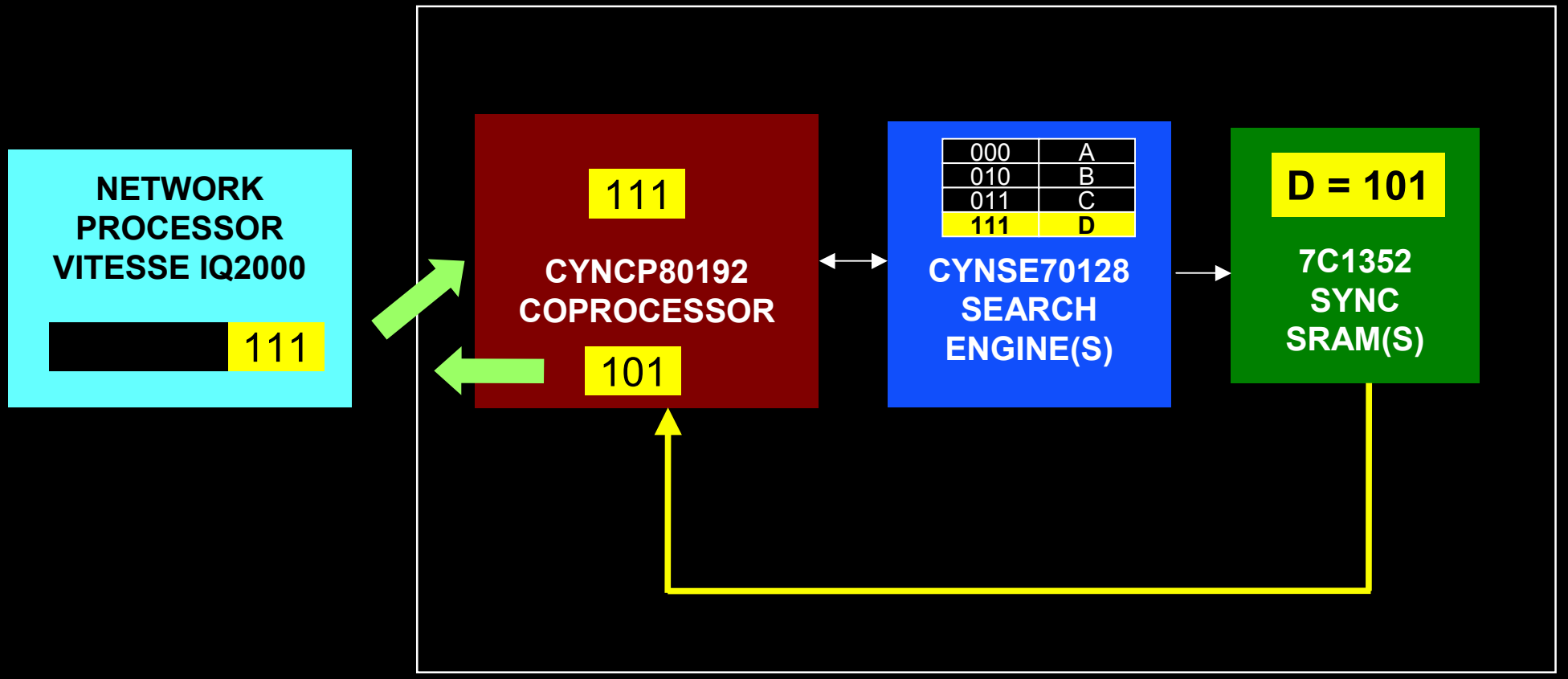
PARTNERS: NORTEL, CISCO, RIVERSTONE

POSIC2GVC


16 CHANNELS
DYNAMIC ALLOCATION
GE OVER SONET
FC OVER SONET
ESCON OVER SONET

PROBLEM: PACKET FORWARDING AT OC-192 SPEED

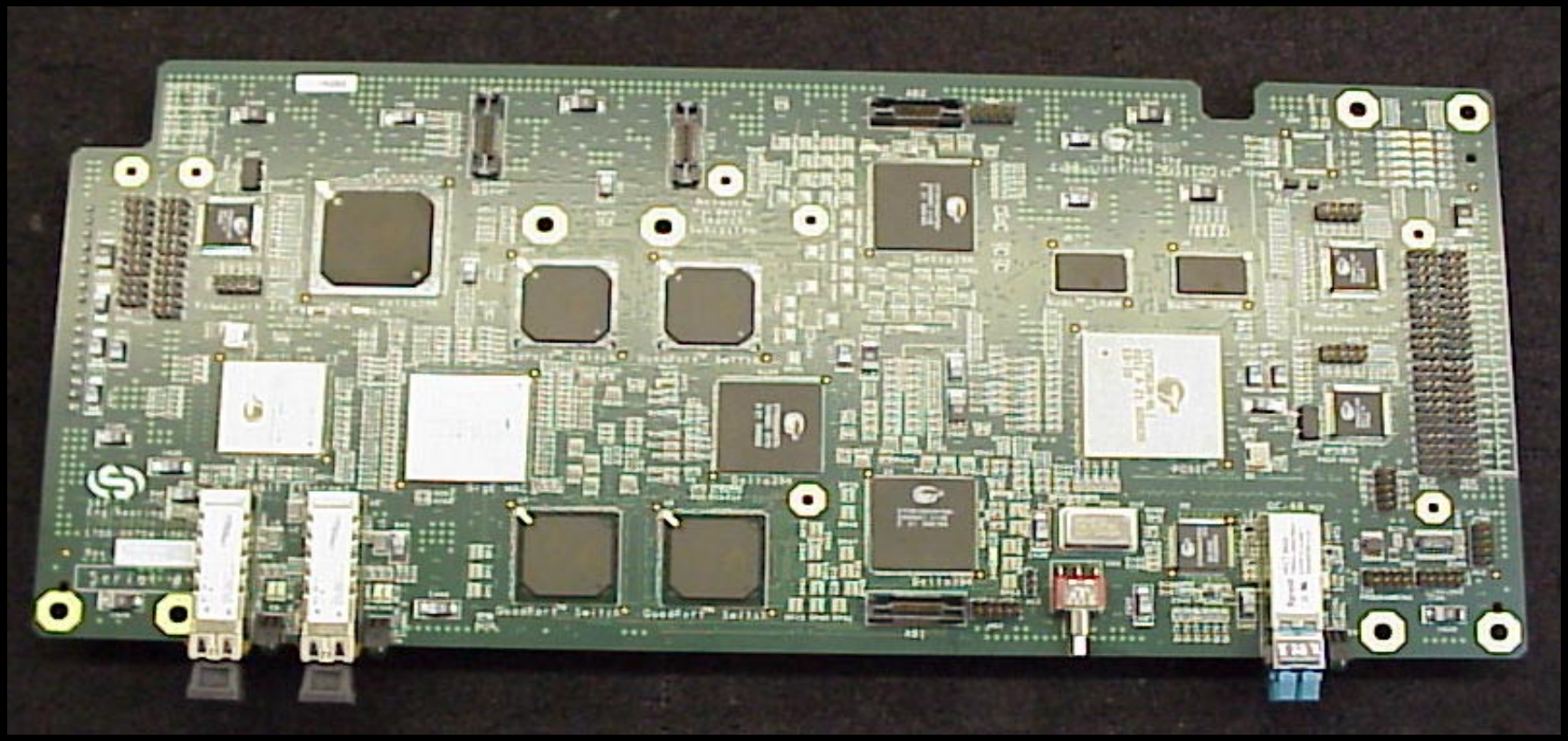
NETWORK SEARCH ENGINE



PARTNER: CISCO

256K NSE

CYPRESS OC-48 / STM-16 LINECARD

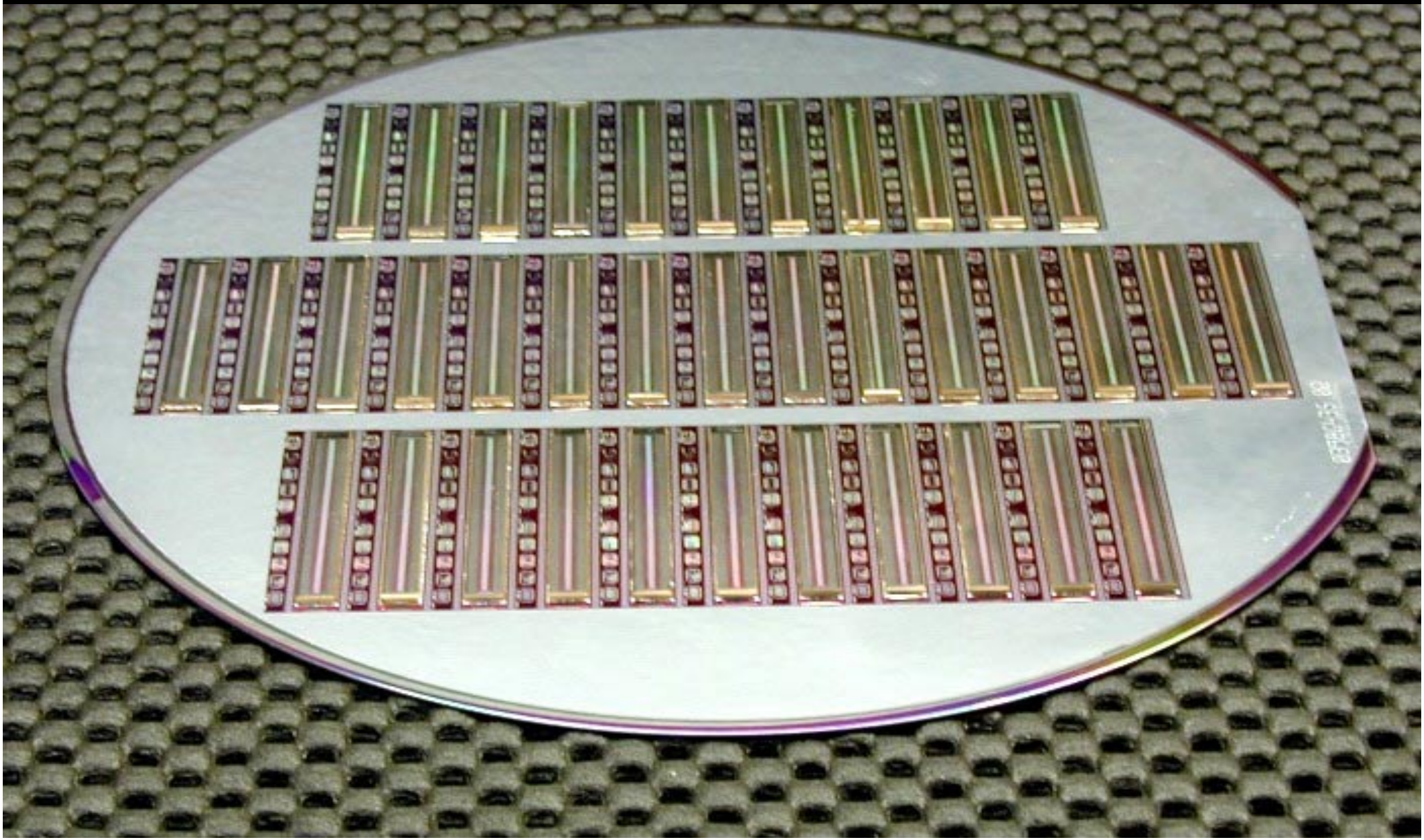


OC-48 SYSTEM SOLUTION

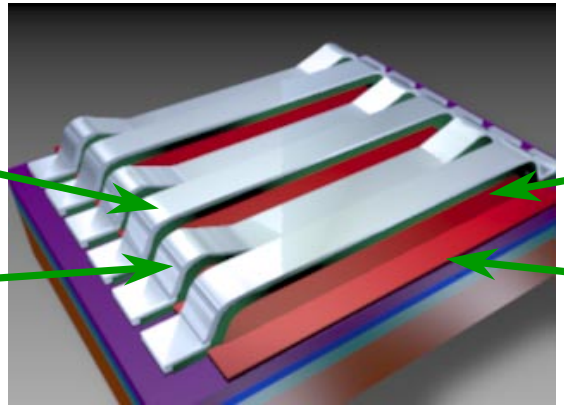
FUNCTIONS
- 2 X GIGE BACKPLANE
- LAYER 3 CLASS
- LAYER 4 CLASS
- OC-48 PORT

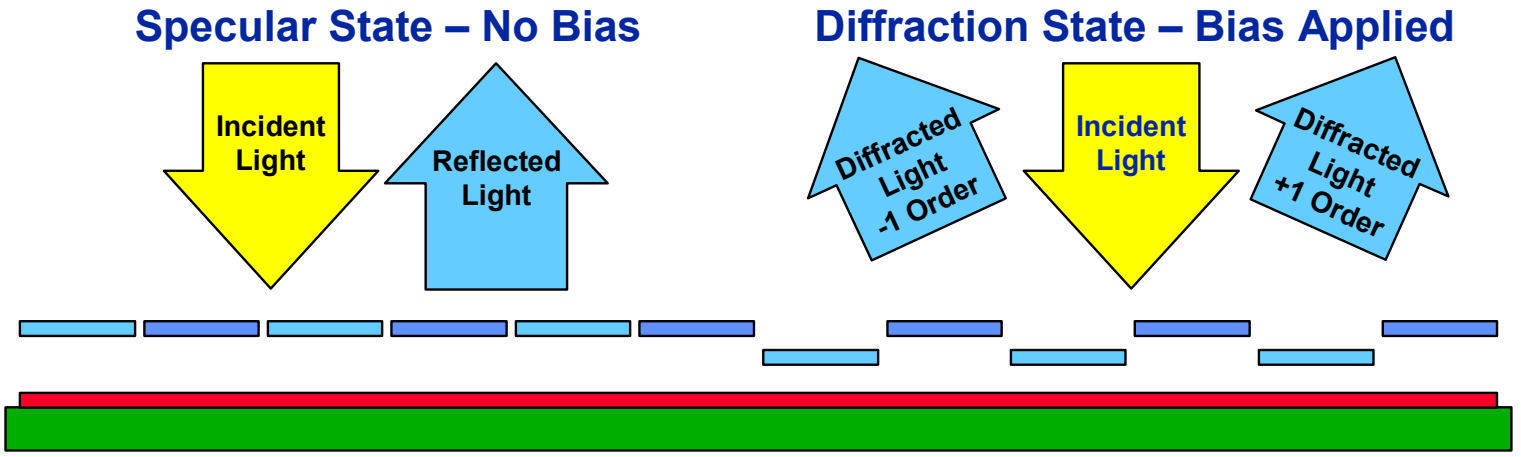
ALL CYPRESS SILICON
- DCD (POSIC™ FRAMER, OC-48 PHY, HOTLINK II™ PHY, QUADPORT™ DSE, DELTA39K™ CPLD)
- MPD (NOBL™ SRAM)
- TTD (ROBOCLOCK II™ CLOCK DRIVER)
- PCD (USB FX-2)
- CMS (PSOC™)

CYPRESS TEXAS DGE WAFER



Grating Light Valve™ Technology
Spatial Light Modulation Based on Diffraction



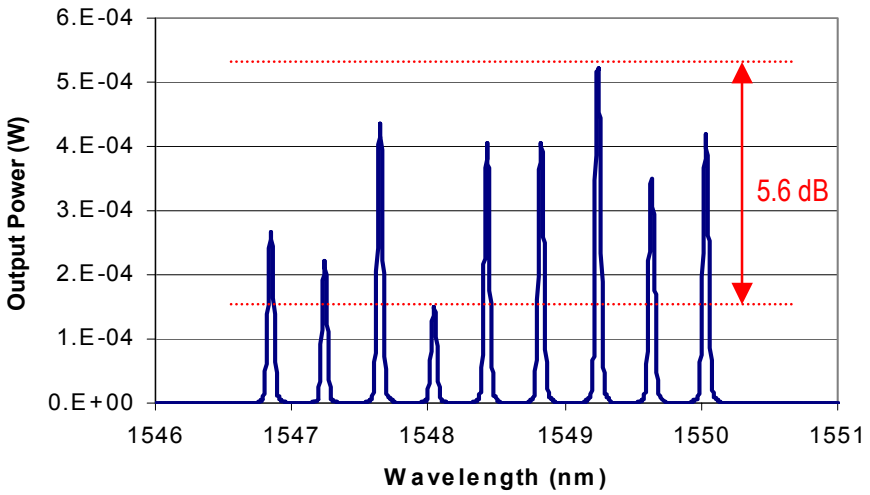


PROBLEM: NON-EQUAL SIGNALS IN DWDM SYSTEM

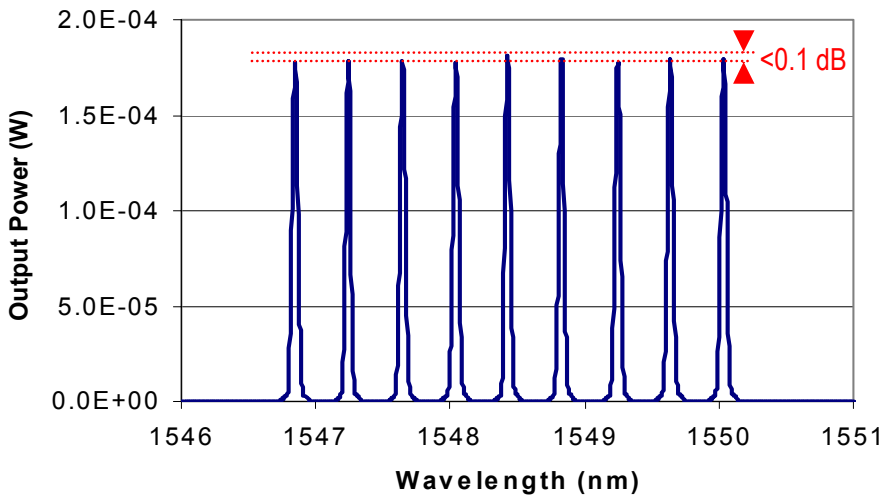
Equalizes DWDM Channels

50 GHz Channel Spacing

Before Equalization



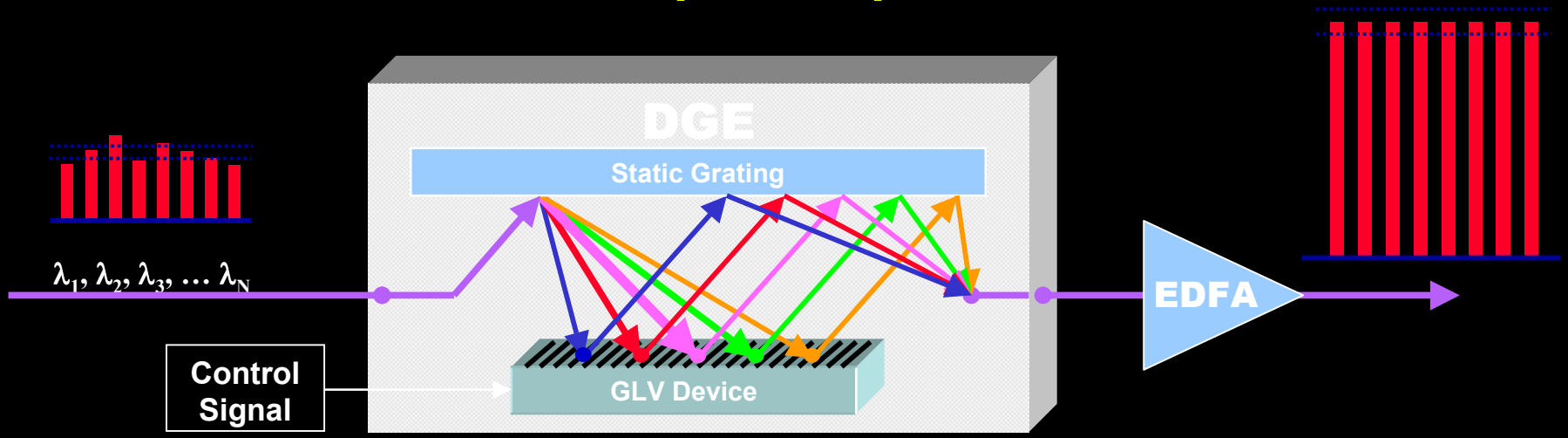
After Equalization

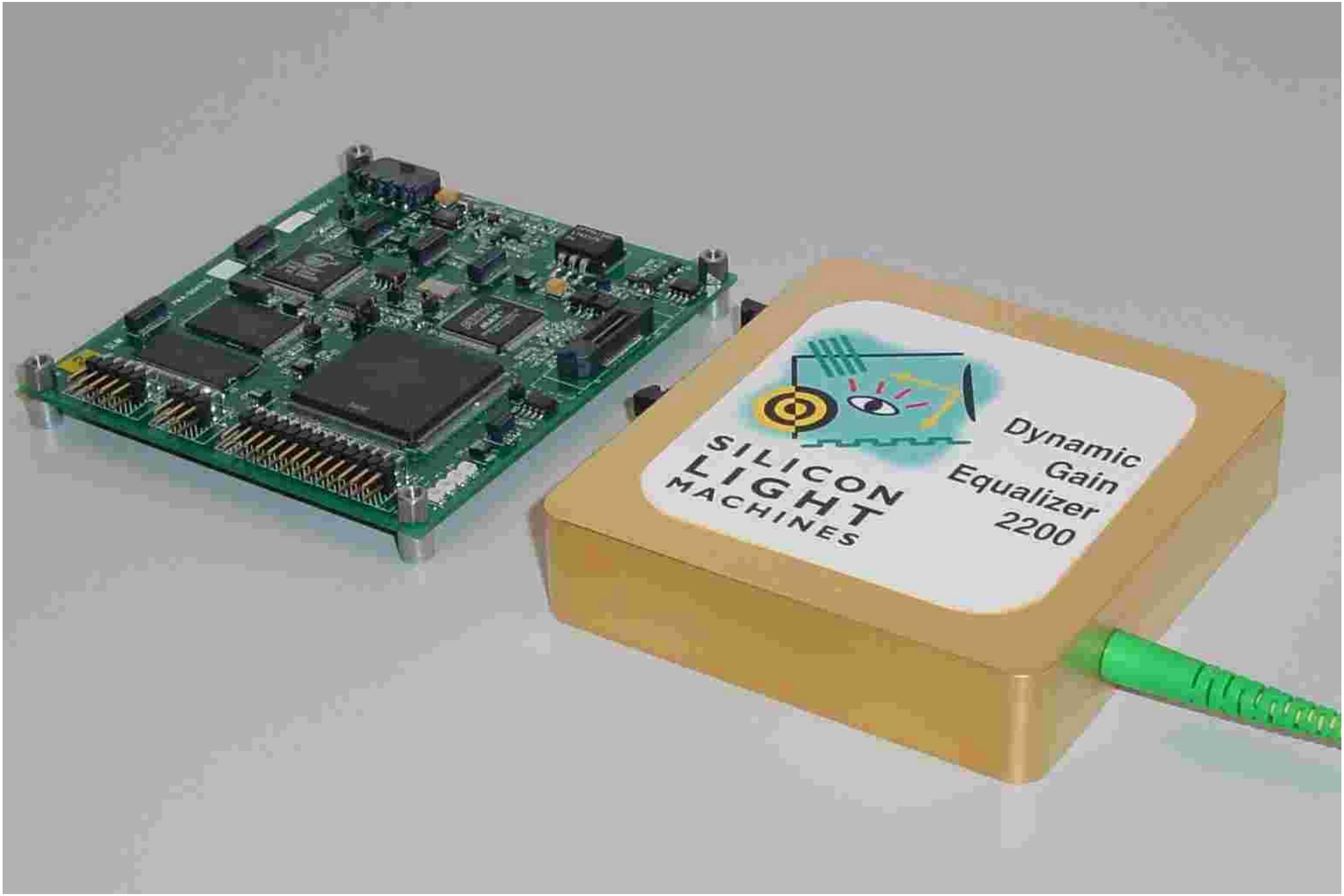


PARTNER: LUCENT, CIENA

SLM 2200 Dynamic Gain Equalizer

Principle of Operation




SILICON
LIGHT
MACHINES
Dynamic
Gain
Equalizer
2200

Highly Accurate Dynamic Gain Equalizer Controls Optical Power Precisely

Based on Grating Light-Valve technology, this versatile MEMS product provides speed, accuracy, and reliability advantages to communication system designers.

Roger Allan Executive Editor

An optical dynamic-gain equalizer (DGE) for dense wave-division multiplexing (DWDM) communication systems sets unprecedented performance levels for precision, dynamic range, and reliability. This product, essentially a seamless one-dimensional array of variable optical attenuators (VOAs), is the first such device to employ diffractive micro-electromechanical system (MEMS) technology with ultra high-spectral resolution. Its maker, Silicon Light Machines, a subsidiary of Cypress Semiconductor Corp., uses a patented MEMS Grating Light-Valve (GLV) technology developed at Stanford University in California, and now optimized for telecommunications applications.

Essentially, a GLV is a diffraction-type spatial light modulator that's fabricated in a standard CMOS fabrication facility. The model 2200 DGE delivers power accuracy, or residual ripple of ±0.1 dB,

tional communication channel that's used affects the shape of the power spectrum. These issues are magnified in dynamically changing DWDM systems.

This is where the model 2200 shines. Designed for C-band operation in the 1550-nm spectral region, it independently attenuates optical power over multiple spectral regions, using a single dynamic module instead of a static approach. Future versions are being considered for operation in the L and S bands.

The 2200 is really a subsystem made up of the drive electronics on a board, an optics module that contains the GLV device, and an opti-

THE PARTNERSHIP DEAL

SILICON SUPPLIER	SYSTEM MAKER
"FREE" IP & DEBUG	YOUR IP IN SILICON
HIGHER VALUE PRODUCTS	MOORE'S LAW: COST, INTEGRATION
DESIGN WINS	PRODUCT YOU WANTED/KNOW
STEADY BUSINESS	STABLE SUPPLY
HIGHER MULTIPLES	HIGHER MULTIPLES

FROM NOW ON: IT WON'T EVEN TAKE A NEAR-DEATH EXPERIENCE TO WORK TOGETHER